Wafer-Scale 3D Integration of InP Membrane Nanophotonics with InP HBT Electronics for Advanced Datacenter Applications

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Salim Abdi

PhD Thesis

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PROEFSCHRIFT

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Thesis Cover frontside: cross-section of a semiconductor optical amplifier. Backside: on-chip electrical interconnects

Dedicated to my family.

Summary

The prolific use of the internet and the high-performance computing needs for artificial intelligence are driving the exponential growth of datacenter traffic. This increases requirements for versatile higher-speed data communication beyond 800 Gb/s and at energy consumption below 5pJ/bit. Vertical integration of EICs with PICs represents a scalable method to fabricate full systems-in-package that respond to these requirements. Intimate co-integration of EICs and PICs can be realized via wafer-scale bonding with BCB, followed by lithographically defined interconnects, to offer the highest scalability in terms of fabrication and packaging cost and yield. Moreover, EICs and PICs based on InP are prized for their ultrahigh performance, so using those for this purpose is ideal. This thesis investigates the potential of vertically integrating InP membrane nanophotonics based on the IMOS platform on InP HBT electronic substrates. The goal is to develop high energy efficiency systems-in-package electronic-photonic ICs (E-PICs) that are scalable for mass manufacturing to respond to the abovementioned needs. The thesis outlines several challenges faced by this integration scheme and investigates novel solutions that are key to enabling functional E-PICs.

After providing the context of this thesis in the introduction, the first part focuses on establishing a cohesive co-integration process flow. This is based on multiple facets; an analysis of the thermal and mechanical compatibility of electronics with the integration approach, development of multi-layer coatings for safe wafer removal, and an improved bonding process to preserve the alignment and bond uniformity. Moreover, co-design rules are set based on fabrication, thermal, optical and electrical considerations to design functional E-PIC circuits.

Next, a new bonding process was introduced to improve post-bond alignment and bond uniformity while leveraging the reflow capacity of soft-baked BCB for void-free bonds. The process combines hard BCB anchors with the soft BCB to achieve the abovementioned characteristics over a wide range of BCB thicknesses relevant to 3D integration. The resulting bonding interface is uniform in terms of optical and mechanical properties.

Adhesive bonding results in wafer-scale membrane distortions. These were analyzed using e-beam metrology. Analysis shows linear expansions of around 300 ppm when bonding InP to other substrates but negligible expansion for InP-to-InP bonding.

Residual distortions are minimal and can be compensated for to enable high throughput scanner lithography on IMOS devices.

To improve the performance of active devices for 3D integration, a thermal management study was realized. DFB lasers using thick thermal shunts were developed to enhance heat removal from the diode by connecting them to the cooled substrate. This improved the device performance metrics like SMSR, WPE, I_0, η_0, and R_{th} compared to reference devices. These shunts were also used to demonstrate polarization-insensitive O-band SOAs with good energy efficiency resulting from high net gain at small current densities while maintaining low polarization sensitivity. Moreover, improved power handling in UTC PDs with enhancements in responsivity and bandwidth were demonstrated using these shunts. The approach also supports lower RF transmission losses in CPW lines and aligns well with the cohesive co-integration process flow.

Based on these developed technologies, a hybrid E-PIC module was co-designed by integrating UTC-PDs with HBT drivers. The design layout and wafer assembly targeted accurate on-wafer measurements and maximizing the yield of co-integrated E-PICs.

Finally, the thesis is concluded by summarizing key results from each chapter, followed by an outlook highlighting further insights and future improvements of these methods within a larger view considering the full 3D system-in-package. This includes insights into improvements of the IMOS platform and devices therein, the 3D integration method, and packaging considering the challenges raised by these complex E-PICs.

Contents

Chapter 1 Introduction

This chapter provides the foundational context for this thesis. It begins by exploring the role of optical communication in our modern society and discusses current data traffic trends alongside future demands. The implications of these trends on the development and performance of commercial devices are then examined. Subsequently, the chapter introduces different concepts for electronic and photonic integration, emphasizing their significance in addressing emerging challenges. Next, an overview of state-of-the-art indium phosphide (InP)-based photonic and electronic devices is presented, focusing on those relevant to the scope of this work. Finally, the chapter concludes with a detailed thesis outline, introducing the key research questions and summarizing the answers as structured across subsequent chapters.

1.1 Optical communication

The world today is characterized by a relentless exchange of information driven by the explosive growth of digital services such as the Internet of Things, e-commerce, and video streaming. By 2024, the global data volume generated by humans and machines then transmitted across the globe has reached several zettabytes, with projections expecting a soaring rise to 400 zettabytes by 2030. [1], [2]. This trend is further amplified as we enter the artificial intelligence/machine learning (AI/ML) era that are already driving transformative changes across multiple industries and applications, from autonomous vehicles to predictive analytics. To keep pace with future global network demands, substantial resources are being invested in reshaping the optical communication landscape and improving the performance of current data centers. The aim is to improve the energy efficiency, speed, and reliability of future commercial devices while maintaining cost-effectiveness, minimal physical footprint, and optimized power usage per function [3].

The single-mode optical fiber lies at the heart of modern optical communication. It enables data transmission with low optical propagation losses (<0.2 dB/km) across specific infrared wavelength ranges, particularly the O-band (1260–1360 nm) and C-

band (1530–1565 nm) [4]. At the two ends of the fiber, pluggable transceivers perform light generation, modulation, and detection through electro-optic components integrated within a single photonic integrated circuit (PIC). These PICs are predominantly based on Indium-Phosphide (InP) III-V semiconductors for active photonic devices, which are chosen for their superior optoelectronic properties.

The exponential growth in data traffic has driven advancements not only in fiber performance and complex modulation formats, but also in the development of more sophisticated PICs, especially over the past decade. Since first reported in 1969 [5], the PICs field has experienced rapid evolution similar to the trajectory of complementary-metal-oxide-semiconductor (CMOS) electronics under Moore's Law [6], [7]. This progress has encompassed the development of individual building blocks as well as density scaling of devices per chip. As a result, integrated photonics has become a cornerstone of the optical communication industry, with mature technology nodes and increasingly intricate circuits, enabling a steady increase in transmission capacity. Furthermore, the democratization of the PIC technology through open foundries and design platforms, as well as the lower cost via multi-project wafer (MPW) runs, is positioning PICs for widespread adoption across diverse applications beyond their wide use in datacenters [8].

For datacenter applications, the data capacity per chip has doubled on average every 2.2 years, and is targeted to continue at this rate to reach capacities beyond 800 Gb/s and at energy consumption below 5pJ/bit [9], [10]. Future requirements are putting higher strains on the industry, which is shifting towards more complex paradigms such as co-packaged optics (CPO). Unlike traditional pluggable modules, CPO integrates optical modules directly onto the substrate where the switch application-specific integrated circuit (ASIC) is attached. This reduces the electrical interconnects length and effectively addresses issues on signal integrity, cost per bit, low wiring density from ball grid arrays, and bandwidth density [2], [11], [12]. For instance, early implementations of CPOs offer energy per bit in the 5-10 pJ/bit range, which is a twofold improvement compared to pluggable transceivers [13]. The network capacity is also increased by a factor of two with a 64% reduced number of switches [14]. This approach has gained traction among major data center builders. However, optimizing the packaging strategy for CPO remains a topic of ongoing industry discussion and development [15]. Here, the fixed configuration of CPO modules can be limiting. Additionally, integrating optical components on the same package requires advanced packaging techniques and careful thermal management to ensure optimal performance [13].

One of the critical bottlenecks for CPOs is the interconnects between PICs and electronic integrated circuits (EICs). All commercial PIC devices require to be interfaced with EIC drivers. So bandwidth scaling and energy efficiency are also affected by the interconnects in between [16]. Methods for integrating PICs with EICs are detailed in Section 1.2. Current methods used by the industry rely on side-by-side assembly during packaging. These are mature technologies, but have inherent limitations in terms of footprint density and bandwidth scaling, especially for applications heavily relying on these metrics such as CPO. Ultimately, the roadmap to enable high bandwidth and bring the fiber fully to the ASIC culminates with vertical/3-dimensional (3D) integration of PICs on EICs [13], [17], [18]. This approach is promising both for pluggable transceivers and CPO technologies. It offers the most effective solution in terms of interconnects distance, reaching unprecedented lengths below 20μm. This applies to all of the chip

interconnects beyond the first row of bump pads as in side-by-side assemblies [16], [19], [20], [21]. Moreover, above chip-level integration, packaging presents another critical bottleneck in terms of technology development and throughput. The assembly of PICs and EICs into functional and commercial-grade systems-in-package (SiPs) is both cost-intensive and time-consuming. Packaging and testing costs share up to 70% of the total cost of commercial devices [22]. Wafer-scale 3D integration of PICs and EICs offers the inherent advantages of 3D integration while significantly improving the packaging throughput and cost accessibility. For this method, the interconnects are fabricated on the wafer scale with one lithography step, eliminating the need for assembly on the chip scale. This method is detailed in Section 1.2.3, and further developed in Chapter 2.

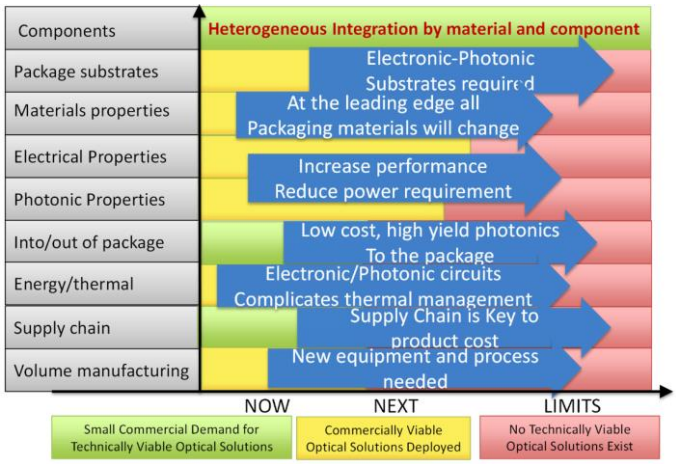

Figure 1.1 Photonic systems packaging roadmap, taken from [3]

Furthermore, to guide research and development of scalable solutions based on PICs, Figure 1.1 presents the roadmap for packaged photonic integrated devices, as outlined in the *Heterogeneous Integration Roadmap: Integrated Photonics Chapter, 2023* by IEEE [3]. It highlights key advancements necessary to sustain the above-mentioned trends. For PIC and EIC components, the goal is to develop high-speed and energy-efficient devices that perform well in datacenter requirements to reduce the energy-per-bit and scale the bandwidth. For packaging, the goal is to decrease the physical interconnect distance between photonic and electronic devices to improve their connectivity and performance. Thus, combining 3D integration with high-speed and energy-efficient devices aligns well with these roadmap objectives.

1.2 Electronic photonic integration concepts

There are several methods to connect PICs to EICs. These are described here with their major advantages and challenges highlighted.

1.2.1 Monolithic integration

Instead of having two separate photonic and electronic ICs, monolithic integration relates to the front-end fabrication of both device types on the same substrate via

epitaxial regrowth, as shown in Figure 1.2.a). For electronics, the maturity and scale of the CMOS technology provide energy-efficient circuits with the lowest cost and highest volume. A promising approach is integrating Si photonics (SiPh) directly in the fabrication processes of CMOS nanoelectronics or bipolar CMOS (BiCMOS) devices to fabricate monolithic electronic-photonic integrated circuits (E-PIC). Many complex systems on a chip (SoCs) have been demonstrated based on this method (see Figure 1.3.a) [23], [24]. Interconnecting the two device types also benefits from the CMOS back-end metal interconnect process [23].

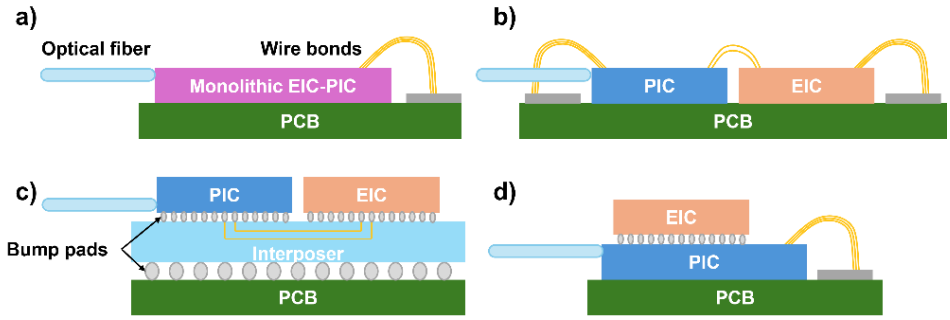

Figure 1.2 EIC-PIC-in-package integration approaches: a) monolithic integration, b) 2D integration using wire bonds, c) 2.5D integrations via flip chip bonding through an interconnecting interposer, d) 3D integration. Adapted from [12]

However, several barriers need to be surmounted for this to be viable for optical communication. For instance, research on direct bandgap materials on Si has advanced significantly using both group IV and III-V materials [25], [26], but efficient monolithic lasers on Si are yet to be demonstrated. Another promising platform that could host this integration concept is the InP platform, which offers high efficiency PIC and EIC devices, as discussed in Section 1.3. However, this will require performance compromises and significant processing efforts as photonic and electronic devices have different epitaxies, processing, fabrication tolerances, and dimensions [27]. As an example, some photonics fabrication steps can be detrimental to III-V EICs device performance as discussed in Chapter 2, and BiCMOS EICs as discussed in [21]. Moreover, in terms of layout allocation, this integration scheme features devices that are integrated laterally in a side-by-side manner. This constrains the SoC footprint and requires further considerations into the thermal and electrical crosstalk between devices on the same chip that exacerbate these constraints.

1.2.2 Die-scale 2D and 2.5D, and 3D integration

The majority of commercial PIC technologies fall within this category. It encompasses the hybrid integration of fully fabricated and diced EIC and PIC chips coming from different technologies. It is split into three major schemes depending on the level of integration. The first is 2-dimensional (2D) integration represented in Figure 1.2.b), where EICs and PICs are mounted onto a printed circuit board (PCB) and interconnected through mm-scale wire bonds. These wires limit the bandwidth by introducing additional parasitic induction effects. They are also not scalable for a higher number of active elements due to the wiring complexity and real-estate limitations, as

will be further discussed. Thus, the 2D scheme does not support the scalability required for co-packaged optics [2], [11], [28].

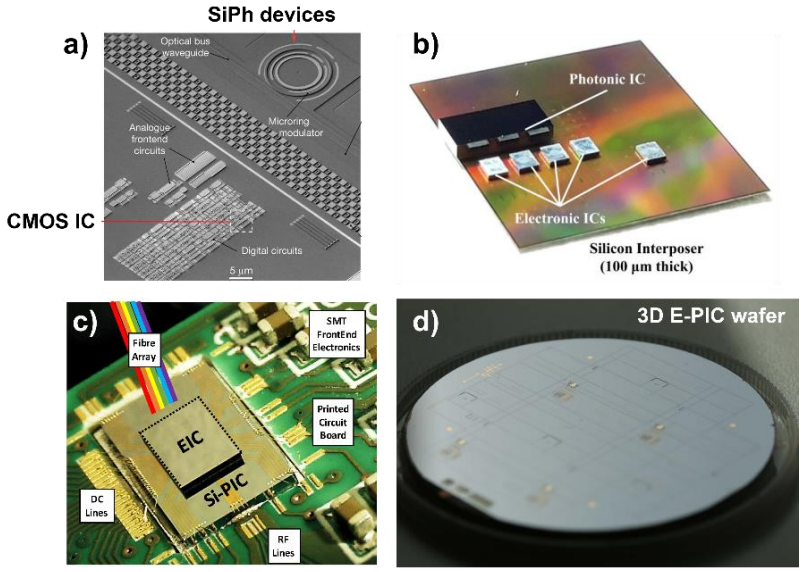

Figure 1.3 a) Angled-view SEM image of a monolithic electronic-photonic microprocessor [23], b) Si interposer connecting a PIC to several EICs [12], c) Image of an EIC on top of a PIC realized during packaging [29], d) Image of a wafer-scale 3-inch InP photonic wafer bonded onto a BiCMOS wafer [21]

The second method is 2.5-dimensional (2.5D) integration illustrated in Figure 1.2.c), where the EIC and PIC are side-by-side flip-chip integrated through solder bumps onto an interposer. The latter acts as a redistribution layer (RDL) that contains all of the interconnections to the two ICs. An example of this method is shown in Figure 1.3.b. Compared to the 2D approach, these interconnections maintain better radiofrequency (RF) signal integrity. However, matching the EICs and PICs to the interposer layout requires additional co-design effort and limits density scaling to the constraints of the interposer, such as using large bump pads [7]. Both methods rely on chip-scale assembly, which limits throughput and cost scalability [22], [16], [30]. However, current efforts for 2.5D integration are focusing on implementing a type of wafer-scale process for assembling multiple ICs on a large interposer wafer that is diced afterward [31].

The third method is 3D integration on the die scale represented in Figure 1.2.d), which is also realized during packaging [32], [33]. This also includes chip-to-wafer 3D integration [34]. Here, one IC (EIC or PIC) is placed on top of the other to achieve low interconnects length. Various types of interconnects are possible, such as metallic bumps and 3D through-silicon-vias (TSVs). This results in lower losses, as the active PIC devices can be designed as close as possible to their driving EICs (Figure 1.3.c) [29], [35]. A compact assembly featuring devices with up to 50 GHz 3dB bandwidth using solder bumps with a diameter of 90µm was demonstrated [36], [37], [38].

However, most devices demonstrated with the 3D approach integrate the EIC on top of the PIC, where active cooling is realized only from the PIC side [22]. This is

problematic as EICs generally dissipate more power than photonics, so their indirect thermal connection leads to several crosstalk problems [39]. The heat generated by EICs can only be efficiently dissipated if they are connected to the packaging heat sink through a low thermal conductivity path, which is difficult to implement from the EIC side in this case [40], [41]. Efficiency in managing the thermal load is especially important not only for preserving the functionality of devices at both interfaces, but also for maintaining the integration density [22], [42]. As an example, thermally sensitive photonic devices need to be placed far away (more than 200µm) from the TSVs to maintain their functionality [42], and this becomes more restrictive for larger thermal loads [41]. Additionally, efficient thermal management for PICs and EICs is especially important for applications in CPOs. This is because of the closer proximity of these ICs to the ASIC which dissipates a lot of heat compared to the case of pluggable solutions where they are placed farther away [13]. This is also because of the stringent requirements in terms of PIC devices raw performance for CPO applications compared to pluggable optics, such as using higher power lasers [43].

A performance comparison of different 2D and 2.5D integration technologies for CPO is provided in [28]. It encompasses the interconnect distance between active EIC and PIC devices, the possible integration density, and packaging costs. 2D integration via wire bonding achieves an interconnect distance of 320µm in the best case. These bonds limit the bandwidth to 100Gbps/channel as a result of their parasitic inductance. Moreover, this short distance is achieved only for the first row of pads while the following rows require longer wires. The second method is flip-chip bonding an EIC on a PIC or *vice versa*. Here, the interconnect length is reduced to 100-150 µm. However, a major disadvantage here is that the interconnect pillars are large, so scaling the number of on-chip active components increases the PIC cost significantly. The bonding throughput here is also limited. Finally, 2.5D integration with a Si interposer is discussed. Here, the interconnect distance is limited by the spacing between the two chips. The smallest interconnect through the RDL is around 300 µm. This limitation needs to be considered for scalability in terms of the number of channels and bandwidths beyond 100Gbps/channel [44].

1.2.3 Wafer-scale 3D Integration

A glimpse into wafer-scale 3D integration is provided here and will be fully detailed in Chapter 2, as it is the core of this work . This approach is mostly in the research phase. It is similar to 3D integration of dies shown in Figure 1.2.d). One major difference is that the entire fabrication flow is realized during the front-end stage in the cleanroom. In detail, a full photonic substrate can be bonded onto an electronic substrate. The photonic substrate is then removed while the electronic substrate becomes the carrier. Then gold (Au) through-polymer-vias (TPV) interconnections are fabricated with one lithography step at the wafer scale (Figure 1.3.d). So all dies within the two wafers are interconnected in one step instead of connecting them per die during packaging, which reduces the price and increases the throughput. Also, realizing this in a cleanroom environment benefits from the quality standards and advanced process control to guarantee high yield and process reliability, such as high precision lithography and dry etching.

Furthermore, bonding these devices close to each other allows for achieving interconnects at unprecedented lengths below 20µm, maintaining the E/O bandwidth and energy consumption of the SiP close to standalone components [45], [46]. However,

this also implies many challenges due to the closely connected electronics that consume a lot of power. So rigorous co-design rules need to be set to control the thermal load dissipation, and electrical and optical interconnects.

The result is an E-PIC similar to monolithic integration (Section 1.2.1), with the advantage that the fabrication processes of PICs and EICs are not compromised, offering more process reliability. Note that some research groups also classify this as monolithic integration because of the similarity in terms of the front-end integration approach [47]. However, an added advantage here is that the PIC and EIC platforms development can be realized independently, then subsequently transferred to the E-PIC design following co-design rules. With efficient co-design taking all considerations discussed in Chapter 2, this scheme allows for higher integration density and more design freedom at the EIC-PIC interfaces relative to monolithic integrations. This potentially opens more opportunities for unprecedented SoCs [10], [20], [48], [49]. For example, 3D integration of high-speed InP double hetero-junction bipolar transistor (DHBT) electronics on BiCMOS Silicon-Germanium (SiGe) electronics enabled hybrid electronic SoCs with superior RF performance than BiCMOS EICs [50]. Recently, a process on SiPh compatible with 3D integration on electronics enabled ultralow-noise lasers [19]. Also, this concept has been previously investigated within TU/e by integrating generic InP photonics on Si BiCMOS wafers. It showed promising results with few setbacks [16]. So the approach was investigated as the core of the *EU TWILIGHT* project using high-speed InP EICs and PICs, and is the main motivation of this work [10].

1.3 InP-based electronic and photonic devices

1.3.1 Electronic devices and circuits

Semiconductor-based RF analog devices saw significant progress in the last decade. For such devices, the transition frequency f_T , maximum oscillation frequency f_{max}, and the breakdown voltage BV_{CEO} are used as figure of merits. There are two main technologies for RF analog EICs. The first is SiGe BiCMOS with best performance exhibiting $f_T/f_{max}/BV_{CEO}$ of 505GHz/720GHz/1.6V, mainly limited by the material properties [51]. The second is InP-based EICs, which perform at much higher speeds and breakdown voltage. These devices exhibit f_T/f_{max} values of more than 0.5/1THz, and with breakdown voltage BV_{CEO} beyond 4-5V for DHBTs [52], [53]. InP high electron mobility transistors (HEMTs) fabricated using nodes below 50nm are better in terms of f_T/f_{max} [54], [55], [56].

For data center applications and requirements, InP EICs can capitalize on the ultra-high bandwidth DHBTs to build low power and low latency transmitter (Tx) and receiver (Rx) electronics [57]. Targeting high symbol rates beyond 112GBd in PAM-4 necessitates high bandwidth analog circuits that circumvent Si CMOS analog-to-digital converters and significant digital signal processing (DSP) [58], [59]. For the Tx, the analog-multiplexer (AMUX)-driver can provide large linear output to drive modulators while operating at low powers. For the receiver, a transimpedance amplifier (TIA)-analog-demultiplexer (ADeMUX) can amplify the signals arriving from the photodiodes to improve the signal quality.

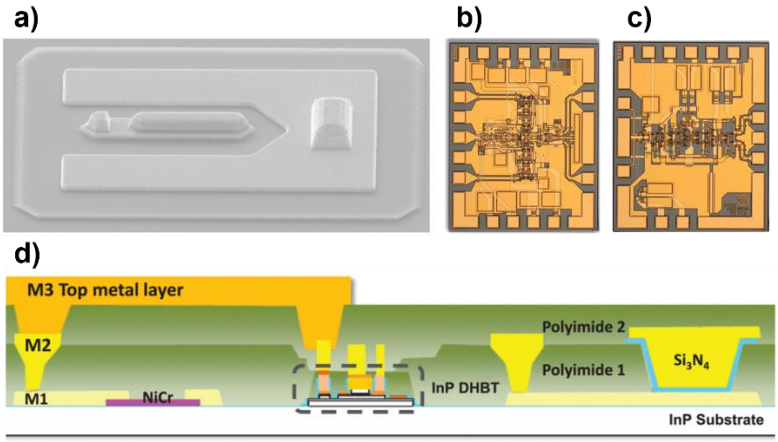

Figure 1.4 a) SEM image of a 0.7×5 µm² InP DHBT. images of: b) InP AMUX Tx driver, b) InP DeMUX Rx IC, d) InP DHBT technology stack for full ICs

The design and fabrication of InP DHBTs within this project is realized by our collaborators in III-V lab. The technology for fabricating 0.7µm and 0.5µm emitter size DHBTs is mature, with the former exhibiting 400GHz f_T and f_{MAX} and BV_{CE0} above 4.5 V, while the latter exhibits higher f_{MAX} of 520GHz [60], [61]. The technology is also advancing toward smaller emitter sizes (<0.4µm) and advanced epistacks to target higher f_T and f_{MAX}. This is realized by lowering its resistance-capacitance (RC) products and improving the total electron transit time [62]. Smaller DHBTs are also more compact and allow for higher integration density, *i.e.*, smaller circuits with lower power consumption.

An angled top-view SEM image of the DHBT structure is shown in Figure 1.4.a). Figure 1.4.d) shows a schematic cross-sectional view of full EICs. It includes Nickel-Chromium (NiCr) based thin film resistors, Silicon-Nitride (SiN) based thin-film capacitors, and Au-based multilevel interconnects. Both Tx and Rx circuits were realized using this technology, with their respective images shown in Figure 1.4.b) and .c). These occupy a footprint of 1.2×1.5 mm². Record values for the gain×bandwidth product were achieved for the AMUX driver with no DSP support, while the ADeMUX requires further development [63]. The Tx EIC was also assembled with Lithium Niobate modulators and generated 100GBd PAM-4 and OOK optical signals, with no DSP support or active cooling [64].

1.3.2 InP photonic devices and membrane nanophotonics

InP-based optical devices have been pivotal in advancing communication systems. To meet the growing demands for scalability in bandwidth and integration density, generic (substrate-based) InP PICs emerged as a versatile solution [65]. These platforms combine active and passive building blocks to allow for higher freedom in realizing complex SoCs in a monolithic manner [8], [65]. This is because all active and passive optical functionalities are realized in a single chip with no partitioning, so coupling losses and parasitic reflections are significantly reduced [7]. Electrical interconnects are also not partitioned, thereby retaining the layout design freedom for optimal performance while offering reduced footprint by eliminating large bond pads for chip

interconnects. Hence, the circuit density and functionality of InP PICs significantly improved, featuring up to thousands of components per chip [65], [66].

The same monolithic functionality can be realized on an InP membrane, similar to the SiPh platform [67]. We refer to these components as membrane devices since they are fabricated on a micrometer-thick epitaxial layer suspended on a low-index material [68]. Here, the mode-size reduction is granted by the high index contrast, so devices can be effectively miniaturized, which is key to scalability [69], [70]. Indium phosphide membrane on silicon (IMOS) as a nanophotonic platform is an example of a platform offering this type of devices. It retains the advantage of native active devices from the InP material system, and also offers an order of magnitude higher scalability of energy and footprint relative to the generic equivalent [7], [70], [71]. Figure 1.5 shows a schematic illustration of IMOS membrane devices interconnected with EICs that form the carrier wafer.

To detail, IMOS devices are realized on a thin membrane epi-stack with thickness ranging from 0.3-2μm depending on the devices included. Some device processes are realized before bonding, such as the deposition of contact metals for semiconductor optical amplifiers (SOAs). The membrane is then bonded onto the carrier substrate using a benzocyclobutene (BCB) adhesive polymer. This carrier can be either blank or contain driving electronics. The fabrication subsequently continues on the fresh atomically flat topography after bonding. Compared to generic processing, this double-side process could enable the integration of multiple active and passive devices with a lower number of epitaxial regrowth steps and reduced compromises on performance [72].

For passive devices, IMOS nanophotonic waveguides (Figure 1.5.b) exhibit optical losses of around 10dB/cm for EBL patterning, which is higher than SiN [73] and SiPh [67] platforms. However, the loss can be reduced more than tenfold by using ArF scanner lithography for lower sidewall roughness [68]. All of the passive devices are more compact than in the generic InP platform, such as bends with small radii, multi-mode interference (MMI) devices, and high-efficiency polarization converters (Figure 1.5.c) [74]. Small footprint (0.2mm^2) arrayed waveguide gratings (AWGs) with 3.7dB insertion loss and 15.3dB channel crosstalk were also realized [75]. These are implemented in the initial transceiver architecture discussed in Chapters 2 and 8 for wavelength multiplexing and demultiplexing. Moreover, some devices are only enabled by the tight optical confinement in the membrane like ultra-sharp 90° bends [76], ultra-compact phase shifters (Figure 1.5.d) [77], and photonic crystals.

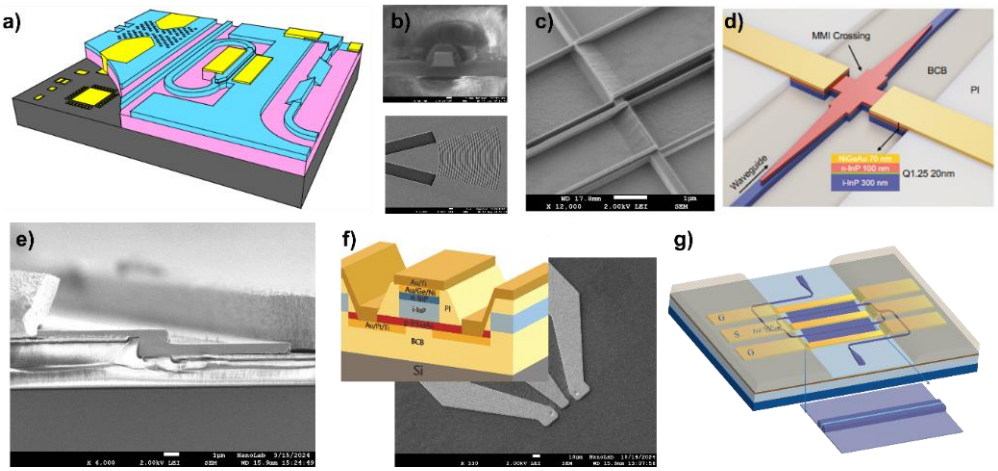

Figure 1.5 Schematic illustration of the IMOS platform, b) top: cross section of an IMOS waveguide embedded in SiO_2 and BCB, bottom: I/O focusing grating coupler, c) polarization converter [78], d) phase shifter [77], e) SOA/DFB, f) UTC PD from [79] and SEM from this work, g) electro-optic modulator [80].

Currently, optical input/output (I/O) fiber coupling to IMOS chips is realized vertically through grating couplers (GCs) (bottom of Figure 1.5.b). These have a typical coupling loss of 5-8dB/coupler, which can be reduced to 1-2dB/coupler using metal reflectors to also couple reflected light [68]. They are polarization sensitive, with a 3dB bandwidth of around 40nm, which can be problematic for measuring broadband devices like SOAs [81]. Edge coupling with broadband polarization-insensitive spot-size converters (SSCs) is being developed, and initial characterization shows promising results [82], [83].

For active devices, IMOS SOAs are based on an S-shaped vertical injection p-i-n structure for optimal electrical injection (Figure 1.5.e) [74]. Optical coupling between these devices and the passive waveguide is realized either with evanescent coupling or butt coupling [74], [84]. Multiple devices were demonstrated with these SOA structures, such as distributed-feedback lasers (DFBs), directly modulated lasers (DMLs), and polarization-insensitive (PI)-SOAs [68], [81], [84]. However, this S-shaped configuration also poses challenges in terms of thermal dissipation and mechanical stresses as will be discussed in Chapter 6. Moreover, compact 3×2 μm^2 uni-travelling-carrier photodiodes (UTC-PDs) with 3dB bandwidth beyond 110 GHz and ultra-low RC constant were demonstrated (Figure 1.5.f) [79]. These PDs implement a butt-coupling scheme to the passive waveguide, which is limiting in terms of power handling. Electro-optic slot-waveguide modulators with 100 nm slot width that exhibit a 3dB bandwidth of 40GHz were realized (Figure 1.5.g) [80]. However, the recent development of IMOS modulators is following footsteps from the generic InP platform configuration, especially since these are compatible with the standard SOA stack. Modulators from the generic platform demonstrated compact co-planar stripline Mach-Zehnder modulators with 160GBd PAM-4 modulation [85].

Additionally, other platforms similar to the principle of IMOS have demonstrated DMLs with 108GHz bandwidth and 0.47pJ/bit energy consumption [86]. At the systems level, ultra-compact and dense circuits on IMOS were demonstrated, such as widely

tunable lasers [87], and 8×8 optical space switches [83]. Moreover, membrane photonics are compatible with 3D integration onto electronics. This will be comprehensively addressed in Chapter 2. Additionally, An added advantage of integrating IMOS devices onto InP electronics is the matching coefficients of thermal expansions (CTEs) for the two substrates, which reduces strain and long-term damage compared to integrating InP on Si BiCMOS, as discussed in Chapter 4. All of these characteristics highlight the potential of InP membrane devices for future PIC development and realization of complex SoCs [74].

1.4 Thesis outline

This thesis focuses on developing 3D integrated membrane photonics for high-speed applications. The study was part of the TWILIGHT, a European Horizon 2020 project. For 3D integration, it covers process convergence for InP E-PICs and required process and co-design development. For photonic devices, it covers the development of devices targeting high energy efficiency and RF bandwidth via better thermal dissipation and lower polarization-dependent losses. The developed processes are tested in a 3D integration demonstrator with EICs. The thesis addresses the following research questions:

- **Question 1:** Is it possible to combine InP photonics and electronics without performance compromises? Are there any compatibility issues?
- **Question 2:** Can the bonding process be improved to reach the high alignment accuracy and bond uniformity requirements of 3D integration?
- **Question 3:** Does the bonding cause residual stresses and distortions to the membrane? Is it detrimental to fabrication?
- **Question 4:** How can the energy efficiency and RF performance of active membrane devices be improved with better thermal management and using processes compatible with 3D integration? Is the method scalable in terms of footprint?

1.4.1 Thesis structure

This thesis focuses on developing a platform for 3D integration of photonics with electronics by answering these questions. Multiple facets of this integration are discussed in separate chapters. Related published findings are indicated in each chapter. The spectrum of this research is broad and involves collaborations from multiple colleagues within TU/e and partners within the TWILIGHT consortium. So their contributions are also highlighted within relevant chapters. The thesis is organized as follows:

• **Chapter 2** focuses on the development of key processes for 3D integration. It lays out the cohesive co-integration process scheme, and identifies critical steps that require optimization to join PIC and EIC components in a single chip. Additionally, co-design rules for the 3D stack are established based on experimental and simulation data encompassing interconnect fabrication, and electrical, optical, and thermal considerations.

• **Chapter 3** focuses on the development of a novel adhesive bonding process for improved alignment accuracy and bond uniformity. Bonding with soft BCB passes through a reflow step where the wafers shift relative to each other and the bond

uniformity degrades. These characteristics were improved by an order of magnitude by introducing hard BCB micro-pillars that act as anchors during bonding. The anchors become a natural part of the bonding interface resulting in a uniform bond.

• **Chapter 4** turns to study the impact of bonding on wafer-scale spatial distortions of InP membranes, which can compromise fabrication. E-beam metrology was used to investigate these distortions with nanometer-level accuracy. This comprehensive study included bonding using various BCB thicknesses and carrier substrate materials, as well as an analysis of residual stresses and bonding defects impact on distortions. The findings quantify these distortions to help overcome challenges related to multilayer overlay errors in the fabrication of heterogeneous devices.

• **Chapter 5** details the technological development realized for fabricating InP active membrane devices discussed throughout Chapters 6-8. It covers the development of a thermal shunting scheme for membrane devices on BCB. The fabrication flows of SOAs and UTC-PDs with thermal shunts is discussed, detailing important contributions for future reproducibility. Next, it covers the fabrication and results of on-chip semiconductor resistors compatible with the IMOS epi-stack, and ways to accurately design them.

• **Chapter 6** presents an in-depth study on the development of thermal shunts to achieve energy-efficient SOA-based devices as these generate a lot of waste heat. It is also used to boost the power handling capacity of UTC PDs as these catastrophically fail at high input powers because of overheating. The shunt is designed to efficiently dissipate the heat to the substrate, and in the case of 3D integration it also connects the photonics to electronics. Experimental results show significant improvements for the shunted DFB laser relative to reference heat-isolated devices. This method is shown to be compatible with 3D integration and improves the energy efficiency and potential for density scaling for these devices. For UTC-PDs, simulations suggest similar benefits to device performance. DC and RF experimental results validate this, with improvements in DC responsivity, power handling, 3dB bandwidth beyond 67GHz, and RF output power linearity up to high photocurrents.

• **Chapter 7** capitalizes on the improved thermally shunted SOA design to demonstrate energy-efficient polarization-insensitive O-band and C-band SOAs based on a thin tensile-strained bulk active core. Combining the shunt with reduced Auger recombination for the O-band SOA resulted in significant gain at small current injection densities and low polarization dependent gain. The chapter explores the development and characterization of the epi-stacks, fabrication of devices, and experimental results. Finally, the focus shifts to assessing the fabrication tolerance of O-band and C-band GCs used in this work.

• **Chapter 8** focuses on utilizing the technology developed and detailed in previous chapters to demonstrate a full receiver co-integration run. Details of the PIC receiver circuit, availability of PIC and EIC devices, and circuit co-design are discussed. Results and limitations are also provided.

• **Chapter 9** summarizes findings from earlier chapters followed by an outlook highlighting further insights and future improvements of this co-integration technology at multiple scales. It provides insights for improving the IMOS platform, 3D integration method, and packaging considering the challenges raised by these complex E-PICs.

Chapter 2
Wafer-scale 3D integration of InP membrane PICs on InP EICs

In this chapter, we focus on the development of key processes to enable wafer-scale 3D integration of InP PICs on InP EICs at ultra short separation distances (<15 μm) via adhesive bonding. First, we describe the co-integration scheme and focus on key aspects developed within this work, also laying the foundation for technologies developed in chapters that follow. Next we identify the most critical steps and optimize them to achieve high thermal and mechanical compatibility of components. Finally, we analyze a method to selectively remove the InP substrate from the photonics side via wet etching while protecting the InP electronics carrier wafer with hermetic multi-layer coatings. Moreover, the 3D integrated stack design must comply with multiple restrictions, including fabrication tolerances, electrical routing, optical coupling, and thermal management. Hence, we also identify key co-design rules and set the required tolerances that need to be accounted for during the design stages to achieve functional 3D E-PIC devices. [1]

2.1 Introduction

The prolific use of the Internet and the high performance computing needs for artificial intelligence (AI) models are driving the exponential growth of datacenter traffic [1], [2]. This increases requirements for versatile higher speed data communication beyond 800 Gb/s and at energy consumption below 5pJ/bit [10]. However, current transceiver technologies are limited in terms of bandwidth scaling and energy efficiency, with

[1] This chapter is based on the work published in J7, C6, C7, and C13 from the list of publications. For contributions, partners from III-V lab (Dr. Virginie Nodjiadjim and Dr. Romain Hersent) provided the EIC samples and measured them before and after processing. They also provided the power dissipation profile for the InP driver. Jasper de Graaf (PhI group, TU/e) simulated RF losses of coplanar waveguide (CPW) lines.

bottlenecks not only restricted to the EIC/PIC devices, but also to the connections in-between [16]. For current pluggable transceivers, the driving EICs and PICs are mounted side-by-side on PCB and hybrid interconnections are realized through wire bonds. This limits the system's bandwidth due to the RF parasitic losses of long wires and poses packaging constraints as a result of piece part handling [16]. This assembly also requires large footprint that is limited by form factor standards, which is becoming increasingly more constrained for pluggable modules. On systems' level, the industry is trending towards CPO, which is not compatible with the wire bonding approach [2], [11], [12]. Closer integration through E-PICs is becoming increasingly important for both of these technologies.

This 3D integration is promising, especially since ultra-high-performance devices with high downscaling potential can be intimately integrated [88]. Moreover, InP is prized for its exceptional electronic and optoelectronic properties. In electronics, InP offers ultrahigh-speed transistor technologies with frequency cutoffs beyond 1 THz, such as HEMTs and DHBTs, achieving unmatched circuit bandwidths beyond 200 Gb/s [57], [62]. In photonics, InP-based components demonstrated performance exceeding 100 GHz [89], including single modules with over 300 GHz bandwidth [90]. Intimate co-integration of the electronics and photonics layers can be realized with wafer-scale bonding, followed by lithographically defined interconnects, to offer the highest scalability in terms of fabrication, and potentially improving packaging cost and yield.

This chapter focuses on key process development and co-design considerations to enable wafer-scale 3D integration of InP photonics on InP electronics. It is organized as follows. In section 2.2 I introduce the co-integration scheme from the perspective of electronic/photonic devices and optical/electrical connections in-between. In section 2.3 I discuss the fabrication flow and identify its related major challenges. I investigate each of these challenges separately. Next, in section 2.4 I discuss the co-design rules. Finally, I conclude the chapter in section 2.5.

2.2 Co-integration scheme

Figure 2.1.a shows the electrical and optical wiring scheme of the receiver and transmitter sides of a co-integrated TWILIGHT transceiver. Figure 2.1.b shows a false-scale schematic cross-section of the vertical stack with InP membrane photonic devices on top of InP DHBTs, co-integrated in the wafer-scale. Here, membrane PIC devices are bonded with BCB to the EICs and connected with ultra-short (<15 μm) TPVs. The TPVs are lithographically defined at wafer scale [21], allowing for high density interconnects and high assembly scalability in terms of chips per wafer and costs per chip, for given EIC and PIC technologies. So scaling here is mainly limited to the InP wafer size, which is being developed towards 6-inch processing to enable more InP-based solutions [91].

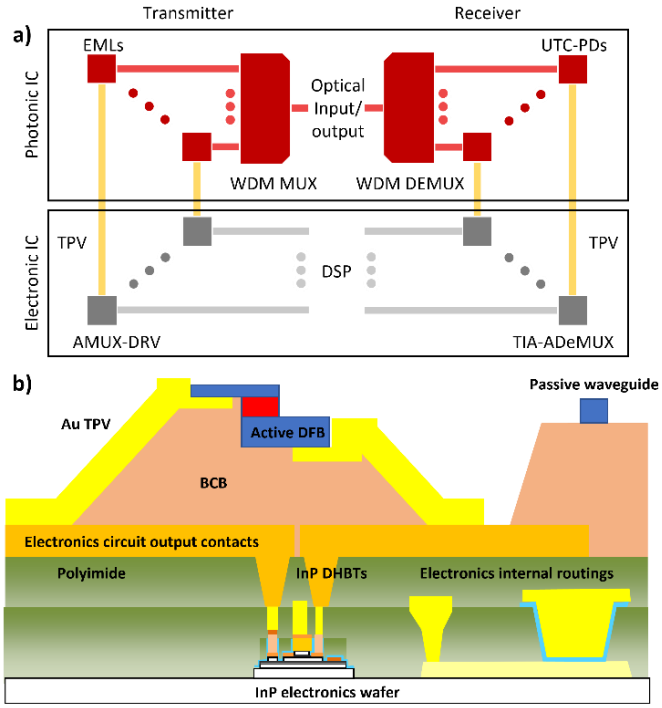

Figure 2.1 a) Electrical and optical scheme of the co-integrated Tx and Rx, b) schematic illustration of the co-integrated E-PIC, dimensions are not to scale.

For this scheme, the optical signal is transmitted laterally between I/Os and photonic components through passive waveguides (light red in Figure 2.1.a). The electrical signal is transmitted vertically between the photonics and electronics with TPV interconnects (golden yellow in Figure 2.1.a) [21]. At the transmitter, an externally modulated laser (EML) generates and modulates the optical carrier. Simultaneously, the electrical signals from the DSP unit are multiplexed to increase the link throughput with an analog multiplexer (AMUX), [64], [92]. The latter monolithically integrates a linear modulator driver (AMUX-driver) to ensure a sufficient extinction of the optical carrier at the transmitter output. Modulated optical signals from multiple transmitters are aggregated through wavelength division multiplexing (WDM). At the receiver, the optical signal is collected and demultiplexed using WDM into separated wavelengths. The latter are detected in multiple high-speed photodiodes. Each are converted into an electrical signal that is transmitted vertically through TPVs to the transimpedance amplifier (TIA)-analog demultiplexer (ADeMUX) to be subsequently re-amplified and demultiplexed before passing through the receiver DSP [20].

2.3 Fabrication flow and challenges

Several technological challenges need to be overcome for successful co-integration of InP E-PICs. In this section, we briefly present an overview of the co-integration fabrication flow and associated challenges with the multiple steps, focusing mostly on those covered by this work. Figure 2.2 shows a schematic illustration of the major steps

related to this flow. For this scheme, we integrate InP DHBTs that are fully fabricated and functional to semi-fabricated InP membrane photonics via adhesive bonding with BCB. This represents a major advantage as the fabrication flow for the photonics and electronics remains similar to the original process with no compromises to each other. The state of these wafers before integration is simplified as shown Figure 2.2.a, with photonics and electronics having topologies of approximately 2µm and 6µm, respectively. All of these fabrication steps are realized on the wafer scale using 3-inch substrates and support scalability to larger substrates.

The integration process starts with preparing the semi-fabricated photonics wafer and the fully fabricated electronics wafer for bonding (Figure 2.2.a). Pre-bond processes for membrane photonics depend on the type of devices, and are described and detailed in Chapter 5 for devices used in this thesis. The integration process involves the deposition and outgassing of 500nm SiO_2 that promotes adhesion of BCB to the substrates. Next, we spin-coat and soft-bake 10- to 12-µm of BCB on the electronics side, targeting a thickness that is close to double the topology on the wafer for better planarization (Figure 2.2.b). As for the photonics wafer, we deposit the SiO_2 layer and follow it with the fabrication of SiN backside markers. Afterwards, we fabricate the BCB anchors, which we pattern by photolithography and dry etching (Figure 2.2.b). We target the same BCB thickness (10- to 12-µm) so that the anchors can reach to the other substrate. The purpose of anchors is to preserve the alignment accuracy and bond uniformity after bonding, as will be comprehensively discussed in Chapter 3. The two wafers are then aligned with the wafer backside alignment method [93], *i.e.*, with front-side markers from the electronics wafer and back-side markers from the photonics wafers, and subsequently bonded in controlled temperature environment (Figure 2.2.c). Here, BCB crosslinks to permanently join the two wafers with a high bond strength and provides low electrical, electromagnetic, and thermal crosstalk between the two interfaces (Figure 2.2.c). A post-bond uniform interface is achieved as both anchors and bond layer are fully baked.

Next, we remove the SiN backside markers, clean the bonded stack from residual BCB, and deposit protective coatings on the backside of the electronics wafer, *i.e.*, the substrate to be preserved (Figure 2.2.d). The latter is realized as the photonics substrate is removed via selective wet etching with an etch-stop layer (Figure 2.2.e). As a result, the etch-stop layer on the photonics side in combination with the backside coatings on electronics side together protect the electronics carrier wafer from damage. Subsequently, the post-bond fabrication of photonics is continued as part of the double-side processing. These steps depend on the type of photonic devices, as detailed in Chapter 5. Finally, BCB is opened in areas near contacts and the PIC/EIC devices are connected with ultra-short TPVs (Figure 2.2.f). This is realized with photolithography and electroplating of Au to reach a thickness in the range of 2-5µm followed by Au seed layer removal with wet etching.

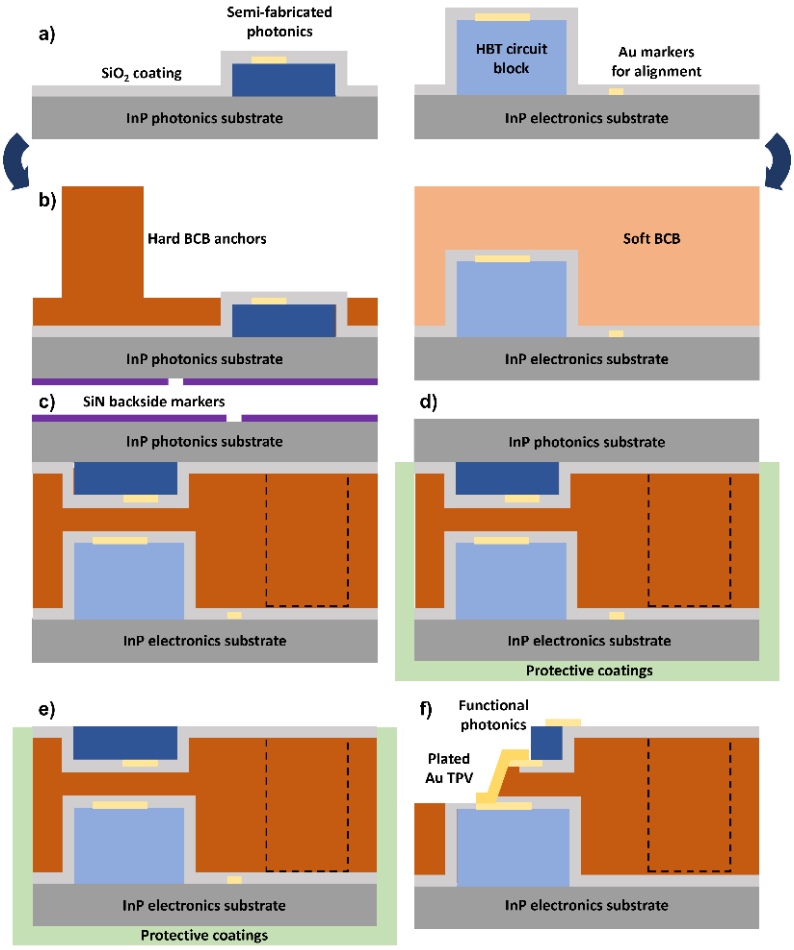

Figure 2.2 Major integration process steps, a) before integration, b) wafers prepared for bonding, c) after bonding, d) deposition of protective coatings, e) photonics substrate removal, f) continued fabrication of photonics, then TPV realization.

The bonding and post-bonding processes are inherent to membrane photonics fabrication, so they do not affect their performance nor add additional fabrication steps [68]. However, these processes were not tested on functional InP electronics. The performance of DHBTs can be affected by the thermal treatments and mechanical stresses introduced during the bonding and post-bonding processes. Bonding is realized at a temperature above 200°C for several hours [93], while other post-bonding steps can be tailored. For instance, SiN hard masks can be deposited at temperatures between 80°C and 300°C using different tools, so low temperature deposition is possible. Hence, an accurate assessment of the thermal tolerance of DHBTs is required to determine their compatibility with this integration scheme, and to define process boundary conditions that respect these limitations. The performance of DHBTs at various thermal conditions, *i.e.*, time, temperature, and ramp-up rate, was studied and is presented in section 2.3.1. Moreover, InP DHBTs are embedded in SiO_2 and BCB after integration (Figure 2.2.c-f). Temperature ramping during bonding causes BCB to

expand at rate that is an order of magnitude higher than InP, which can result in residual stress build-up that affects these devices, or BCB delamination during contacts opening. Thus, a process with low-stress SiO_2 is developed, and assessment of DHBTs performance after opening contacts was conducted. A study on this is presented in section 2.3.2.

After the bonding process, the InP photonics substrate needs to be completely removed to leave only the micrometer-thick epitaxial layer. This is realized with wet etching using concentrated Hydrochloric (HCl) acid over an extended duration and elevated temperature [68]. However, since both of the photonics and electronics wafers are InP-based, the electronics carrier wafer has no chemical selectivity to the solution. Hence, it needs to be preserved with hermetic coatings that cover its backside and edges. InP is very fragile and brittle compared to other substrates such as Si or glass, so defects introduced from HCl attacking open spots and leakage paths can be detrimental to post-bonding processing. The development of low-stress multi-layer protective coatings is discussed in section 2.3.3.

Moreover, a critical point for intimate co-integration of PICs with EICs is to achieve low-loss interconnects benefitting from the short distance. TPV interconnects fabricated using wafer-scale lithography and electroplating have been chosen for this scheme [94]. Their electrical properties will be further discussed in section 2.4.2. As for their mechanical reliability, a study was conducted and reported in [94]. This is because Au is plated at 30°C on top of BCB vias where it is mechanically relaxed, but it has to endure higher temperatures for post-processing during packaging or during operation. Simulations and experiments showed that the mechanical stress on TPVs is lower than the critical stress where these could be damaged for cycling temperatures between -40°C to 100°C. The stress slightly depends on BCB thickness but it is safe for thicknesses below 30μm, which is sufficient for 3D integration.

2.3.1 Thermal compatibility of InP EICs with the integration process

Here, we systematically studied the effects of thermal treatments on InP electronics. For this purpose, high-speed > 350-GHz transition frequency (f_T) DHBTs with 0.7μm emitter width were fabricated at III-V Lab [60] on a 3-inch InP epitaxial wafer. After wafer thinning and dicing into small samples containing multiple DHBTs, as shown in inset of Figure 2.3.b, thermal treatments were carried out on individual samples. The process parameters for integrating, functionalizing, and connecting photonics with DHBTs described earlier require various thermal treatments. These include the bonding process, deposition of oxides and nitrides, dry etching of BCB and semiconductors, and metallization for TPVs. The temperature for most of these processes can be tailored in the range of 80-300°C if required. Hence, values as high as 300°C for short durations need to be investigated to define a safe process flow for DHBTs. This is because the DHBTs fabrication window does not exceed ~250°C [60]. We note that the bonding thermal requirements (time × temperature) is the highest among other processes, which is why the study is tailored for that. So, the temperature requirements tests were realized in EVG520 bonder at vacuum level ($<10^{-5}$ Torr) to mimic the same environment and temperature cure as in real bonding. Guided by the BCB curing requirements, the studied temperature range is 200-300 °C, with ramp rates of 2, 5, and 10 °C/min, respectively [93]. A large range of treatments time was investigated with values of 0.5, 1, 2, 5, 10, and 20 hours. Compiling these 3 parameters yielded 24 distinct process variations, which fully cover all the post-bonding process

parameter space. Note that most of the other post-bonding processes are also realized in a similar vacuum environment at a much shorter time, such as nitride deposition. Thus, their effect could be inferred from this comprehensive analysis in addition to the study on residual stresses presented in Section 2.3.2.

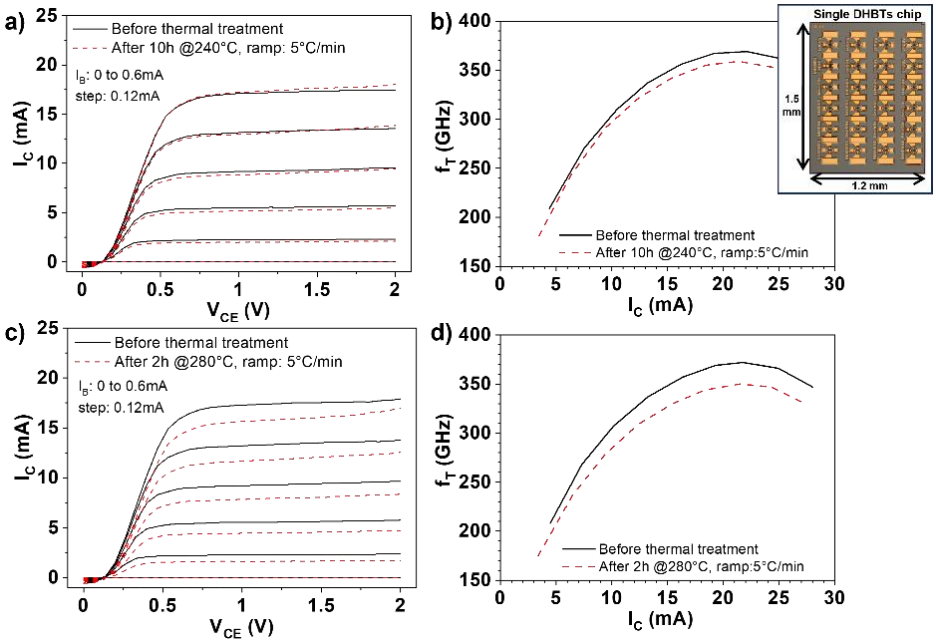

Figure 2.3 a),c) DC, b),d) f_T curves of 0.7x5µm² InP DHBTs before and after baking at temperature, time, and ramp speed of: a) and b) 240°C, 10h, and 5°C/min, c) and d) 280°C, 2 h, and 5°C/min. Top Inset: InP DHBT sample.

The DC and RF performance of the InP DHBTs was measured on-wafer before the thermal treatments and on thinned samples after the thermal treatments. Some DHBTs were also measured on a thinned sample before treatments for comparison. Their DC performance was assessed using $I_C(V_{CE})$ curves, and transition frequency f_T extracted from S-parameter measurements. Results are shown in Figure 2.3. Their post-treatment integrity was determined based on the degree of degradation in their functionality, for example by a variation in their emitter series resistance (R_E) and f_T.

Firstly, it should be noted that the extracted f_T on thinned sample is ≈5% lower than on-wafer measurements, which is due to a small increase of the base-collector transit time likely resulting from additional self-heating effects after dicing. This is taken into account when assessing thermally treated samples.

As a result of the treatments, DHBTs treated at 240 °C (and below) showed identical DC and RF characteristics compared with their pre-treatment performance, regardless of treatment times between 10-20 h and ramp rates between 5-10°C/min, as shown in Figure 2.3.a) and Figure 2.3.b). Treatment temperatures of 260°C resulted in a slight degradation of R_E and f_T for treatment times above 1h. However, samples baked at 280°C for treatment time of 2h significantly degraded, with a 62% increase in R_E and subsequent decrease of f_T, as shown in Figure 2.3.c) and Figure 2.3.d). Devices baked at 300 °C showed significantly degraded f_T, which dropped below 350 GHz, even at

treatment times of only 0.5h. Additionally, we observed no noticeable effect of the ramping rates in our experiments.

Both adhesion SiO_2 outgassing and the bonding process itself are usually carried out at 280°C for 1h [93]. This is to ensure void-free bonding and 100% crosslinking in BCB. Identical results can be achieved with lower temperature of 240°C and longer treatment of 10h as BCB crosslinking requires more time for lower temperatures [93]. However, the process can be optimized for a shorter total cure time. We found that a combination of 2h at 240°C is sufficient for oxide outgassing since we shifted from Plasma-enhanced chemical vapor deposition (PECVD) SiO_2 to inductively coupled plasma CVD (ICP-CVD) SiO_2 that contains less trapped gasses, at detailed in section 2.3.2. For bonding, 9h at 240°C is sufficient for >97% BCB crosslinking. Hence, these parameters were chosen for co-integration. A bonding test with these parameters and optimized protective coatings was then carried out for testing, and void-free bonding was demonstrated.

2.3.2 Effect of SiO_2 and BCB residual stress on the performance of EICs

As mentioned, the DHBTs are embedded in BCB and SiO_2 after the co-integration process. To examine the impact of these additional dielectrics applied on the devices, we tested the performance of 0.7μm InP DHBTs under the presence of residual stress from SiO_2 and BCB. We used two InP cleaved samples containing multiple DHBTs for this purpose. Sample 1 was used to study the stress induced by 500 nm SiO_2 layer, which is required as part of the protection coatings (section 2.3.3). The ICP-CVD SiO_2 layer has a residual stress <100 MPa, measured by the wafer bow method using profilometry discussed in Chapter 3. Sample 2 was used to study the combined stress from 500nm SiO_2 and 12μm BCB deposition, mimicking the stack in the real process. The residual stress of the BCB layer is below 50MPa (Chapter 3). Both SiO_2 outgassing and BCB full cure were performed at 240°C for 10h. To access the contacts and measure DHBTs, contact openings were then defined with photolithography and dry etching in O_2:CHF_3 plasma. Cross-section schematics of sample 1 and 2 are shown in Figure 2.4.a and Figure 2.4.b, respectively. Here, only the probing pad areas are opened, whereas the HBT core is still covered in these layers. Etching of SiO_2 and BCB was done using the same O_2:CHF_3 5:1 chemistry, where etching times of 40 min and 3h30 min were required to clear the layer and reach contacts in sample 1 and 2, respectively.

The number of characterized transistors is 80 before the processing, 26 after SiO_2-only deposition, and 36 after SiO_2+BCB deposition. Superimposed $I_C(V_{CE})$ and $f_T(I_C)$ at V_{CE}=1.6V curves are shown in Figure 2.4.c and Figure 2.4.d, respectively. As shown in Figure 2.4.c), the saturation slopes for sample 1 match the ones before processing and the transistors were not affected by the SiO_2 layer. Measurements performed on sample 2 showed a slight degradation on $I_C(V_{CE})$ saturation slope, which is linked to an average 20% increase in R_E compared to measurements before processing. The same degradation is observed for the 0.5-μm emitter width devices. From Figure 2.4.d, it can be seen that the transition frequency f_T dropped by an average of <5% for sample 2 compared to sample 1 and the data before processing, which was also linked to the increase in R_E.

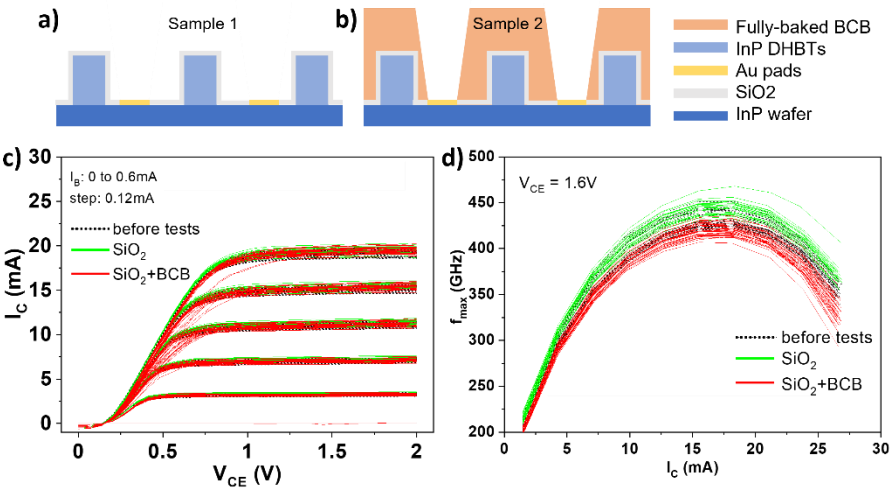

Figure 2.4 Schematic representation of the stacks dedicated for stress tests of: a) SiO_2, b) SiO_2+BCB. Electrical response of 0.7x5 µm² InP DHBTs before and after adding SiO_2 and SiO_2+BCB: c) $I_C(V_{CE})$ characteristics, d) f_T *vs* collector current at V_{CE}=1.6V.

Based on results from the previous section, the total treatment time of 20h at 240°C did not affect the DHBTs performance. Thus, the degradation seen for sample 2 could be related to the extended time required to etch BCB in the reactive ion etching (RIE) CHF_3 plasma process where higher pressure is used, and more investigation is required to further assess this. Moreover, as the DHBTs performance is temperature-dependent, we carried out thermal simulations to assess the temperature of DHBT circuits with/without thick BCB coatings on top (included in section 2.4.4). A difference below 1°C (≈4%) was witnessed between the two cases since most of the heat is dissipated from the substrate through heat conduction. Overall, high RF performance was demonstrated despite this slight degradation. But as discussed earlier, the bonding process was optimized where the outgassing time was reduced to 2h and baking to 9h at 240°C to allow for a larger thermal window to other post-bonding processes.

2.3.3 Protective coatings for low-damage InP substrate removal

Selective substrate removal is a key process to reach the photonics membrane epilayer with precise thickness and without introducing microcracks or defects to the membrane and carrier wafer. Selective wet etching with the assistance of an etch-stop layer is the most commonly used method for this [68]. Etching is done using concentrated HCl:H_2O 4:1 at 35 °C for 1h to remove 650µm of InP. In this InP-to-InP co-integration scheme, the electronics carrier wafer to preserve is of the same material system as the one to be removed. So it requires conformal and hermetic backside protection to block the solution from damaging it while removing the other. Additionally, the gaseous PH_3 by-products generated during etching could lead to further delamination of the protective coating. Moreover, InP is very fragile, so areas attacked by the acid become weak points that can compromise further processing [95]. Thus, low-stress, conformal, and hermetic coatings are needed. Also, the deposition and removal of these protective coatings need to be within the thermal processing window discussed earlier.

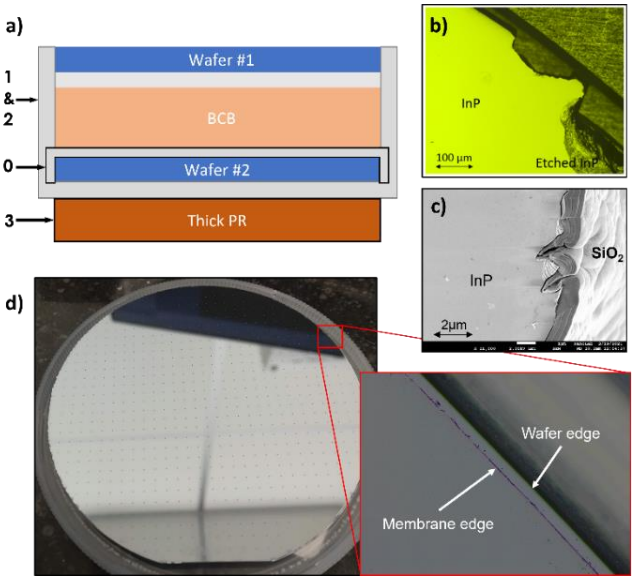

Figure 2.5 Schematic illustration of the layer stack used for protective coatings. L:0-3 indicates the layer number, b) Image from the wafer edge of experiment N#1 c) SEM image of InP wafer edge covered with 1µm SiO_2, (taken by Tjibbe de Vries from NanoLab TU/e), d) image of an InP membrane on InP wafer after substrate removal

Having these considerations in mind, we systematically investigated different combinations of protective layers. A schematic illustration of the tested coatings where wafer #2 is protected is shown in Figure 2.5.a. Table 2.1 shows the experiments realized within this frame. Wafer #1 in these experiments is a bare InP substrate with no epilayers, so it is totally removed after wet etching. This makes it easier to inspect the bonding interface and wafer #2 (the carrier). Layer 0 is the SiO_2 layer used to promote the adhesion of BCB to the substrate, layers 1 and 2 are composed of SiO_2 deposited after bonding to cover the backside and carrier edges. Layer 3 is a spin-coated resist layer that covers the backside for full hermicity.

We first investigated the required SiO_2 (L0) thickness for good BCB adhesion to the top interface of the protected InP wafer (#2) [96]. The tested thicknesses are 50 and 500nm. This was done in the first 4 experiments with 50 nm used in experiment 1 and 3 and 500 nm in 2 and 4. For backside protection, a thick 30µm resist is deposited for experiments 1 and 2, while 3 and 4 also have 1 µm of SiO_2 before the thick resist. The SiO_2 is deposited in ICP-CVD at 80°C and the resist is baked at 110°C. The findings revealed that using 50nm thickness for L0 resulted in BCB delamination near edges during the wet etching, which damaged the underlying InP in exposed spots. Edge defects larger than 100µm were found in experiment 1 (Figure 2.5.b). Using thicker adhesion SiO_2 (L0) resulted in much smaller defects both for experiment 2 and 4 compared with 1 and 3, with experiment 4 having the lowest density of defects. We note that the density here was only qualitatively assessed by optical microscopy. Moreover, the defects are larger in size in experiments 1 and 2 compared with 3 and 4. This is because the 1 µm SiO_2 covers the wafer edge to a good extent (Figure 2.5.c), whereas the thick resist only marginally covers it. Moreover, the backside surface of wafer#2 is fully preserved in all experiments.

Table 2.1 Experimental tests realized to investigate protective coatings. The numbers inside the table refer to the layer number

Exp N	Adhesion SiO_2 (50 nm)	Adhesion SiO_2 (500 nm)	Thin ALD SiO_2 (<100 nm)	Thick CVD SiO_2 (>1µm)	Thick resist (30 µm)
1	0	/	/	/	3
2	/	0	/	/	3
3	0	/	/	2	3
4	/	0	/	2	3
5	/	0	1	2	/
6	/	0	1	2	3

However, from Figure 2.5.c, it can be seen that the 1µm SiO_2 cannot fully cover the micro-cracks on the wafer edge since the deposition is anisotropic. Hence, a <100nm thin SiO_2 atomic layer deposition (ALD) layer was introduced first for conformal coverage [97]. ALD deposition is realized at 200°C. To test if the ALD SiO_2 can fully preserve the backside surface and the edge of wafer#2, we performed experiments 5 and 6. For experiment 5, we used 500nm adhesion SiO_2 on top of wafer#2 and its backside was protected with the ALD SiO_2 followed by 1µm ICP-CVD SiO_2. Experiment 6 includes all layers (L0-L3). For results, the density of edge defects in both experiments 5 and 6 was significantly reduced owing to the conformal coverage of ALD SiO_2, with few small defects of dimensions <10µm. However, the backside surface in experiment 5 contained multiple etch pits with sizes in the 50-100µm range while it remained pristine in experiment 6. This is because the wafers are extensively processed up to the point of bonding, so the backside surface contains more pinholes and scratches, and is contaminated with particles that can detach during the etching process and reveal exposed areas. Hence, the presence of a thick resist layer helps in covering these particles and preserving the backside surface during etching. Both deposition and removal of these coatings are compatible with the DHBTs thermal stability. The resist can be dissolved in acetone at 25°C and SiO_2 can be dry etched at a temperature <200°C. Hence, the combination of protective coatings used in experiment 6 is most suitable for the co-integration. To validate this, we tested the combination again, but with wafer #1 having a ≈1µm epitaxial layer stack. An image of the wafer after substrate removal is shown in Figure 2.5.d. Here, the edge of the wafer is well protected with no visible defects from etching.

2.4 Co-design considerations

The 3D integrated stack must comply with multiple challenges, including low-loss electrical routing, I/O optical coupling, and thermal management. Here, we identify these challenges and set the required tolerances that need to be accounted for during the initial design stages for successful 3D co-integration.

2.4.1 Fabrication considerations

Other than the previously discussed conditions such as post-bond temperature limits, there are other fabrication-related considerations. For opening BCB and creation of interconnects (Figure 2.2.f), an optimal offset between BCB opening and the EIC contact

pads is required. This is because BCB is opened at a slope using AZ9260, at a 1:1 etch rate, *i.e.*, the exact slope transfers from the resist to the BCB. The recipe also etches the EIC polyimide planarization layer as well. So the BCB TPV open mask must be smaller than the EIC Au contact pads to avoid this and ensure a smooth TPV opening. Hence, a sufficient offset from the EIC contact pads mask is required.

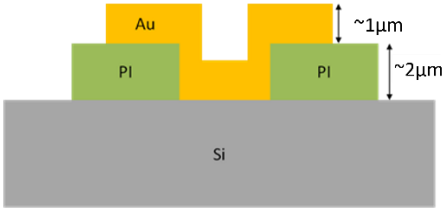

Figure 2.6 Schematic illustration of a Au contact on top of PI used in EICs processing

We tested multiple offsets for BCB opening on EIC pads with dimensions ranging between 50µm to 100s of µm. A test wafer similar in layout to the wafer used for co-integration in Chapter 8 was prepared by III-V lab. It contains only the PI and Au connections required to test the BCB opening process, as shown in Figure 2.6. After etching and inspection, it was found that the optimal offset between the opening mask and the Au pads in the EIC wafer is 15µm. This considers an angle of 37° as a slope for large open AZ9270 areas (Figure 2.7.a), while an angle of 65° needs to be considered for smaller areas around 10µm, like when opening BCB on top of SOAs in Chapters 5-7. This is because the AZ resist height is above 10µm. So its lateral width for values around this height and beyond results in different resist surface to volume ratio. This affects the contact angle between the resist and the layer beneath it during reflow, which is then transferred to BCB during etching. SEM images of an opening on the dummy wafer are shown in Figure 2.7.b.

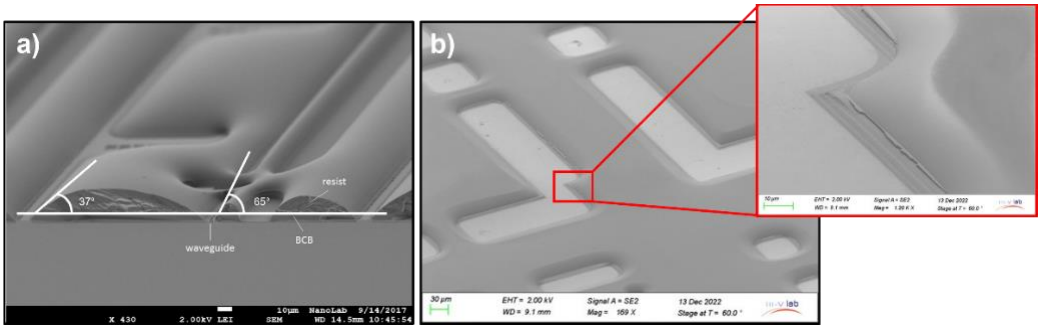

Figure 2.7 SEM images of: a)AZ9270 on top of BCB after etching (image taken by Tjibbe de Vries, Nanolab@TU/e), b) a BCB opening on top of contacts using the right offset (image taken by C. Mismer from III-V lab)

Moreover, since we use BCB anchors for the bonding, the worst-case scenario for post bonding alignment is 10µm, as discussed in the next chapter. This value can be compensated for after bonding for the creation of interconnects. Compensation is realized by measuring the exact misalignment after bonding, then readjusting the interconnections design based on that. Also, note that InP-InP bonding results in no

significant membrane spatial distortions as discussed in Chapter 4. Thus, readjusting optical masks for opening BCB and Au plating only takes the misalignment into account.

2.4.2 Electrical considerations

For optical communication, photonics and electronics are typically designed separately and use a standardized 50Ω impedance to transfer RF signals in-between [94]. To maintain signal integrity, broadband RF interconnects are needed for low parasitics and good impedance matching. For this, TPV and TSV interconnects are superior to bond wires and flip-chip bumps, commonly used for packaging interconnects [98], [99], similar to technologies used for EICs [100]. For instance, heterogeneous integration of InP DHBTs on top of SiGe BICMOS with 3D TPVs in BCB demonstrated hybrid SoCs with bandwidth beyond 300 GHz [50]. Moreover, high density, low parasitic, and break-free Au TPV interconnects connected to coplanar waveguide lines (CPWs) were designed and fabricated. This was realized both on BiCMOS electronic substrates [98], on bare Si, and on n-doped and semi-insulating InP substrates [45]. The BCB thickness used on the BiCMOS substrate was >20µm, while for other substrates it is 7µm, which shows the process versatility. The CPWs and TPVs RF performance was also assessed and 3 dB transmission bandwidth beyond 67 GHz was demonstrated [45], [46], [98], [101]. This bandwidth is mainly limited by the measurement equipment, since the vector network analyzer (VNA) used works up to 67GHz. Note that CPW lines on n-doped InP have much lower bandwidth because of the higher substrate losses [46], but these substrates are not suitable for RF electronic and photonic devices in any case [60], [65].

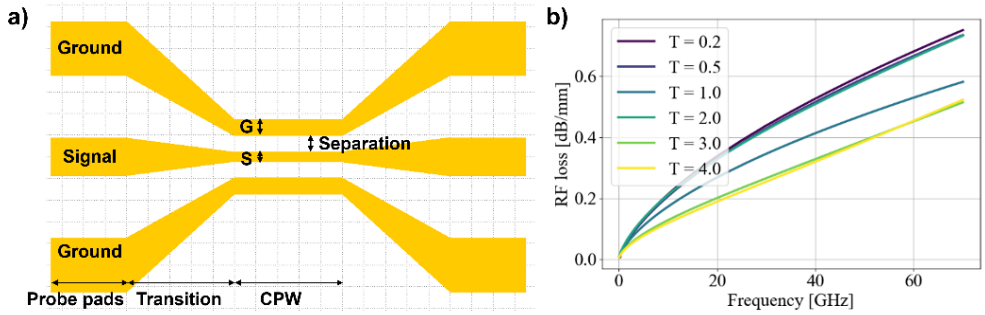

Figure 2.8 a) GDS design of a CPW test structure, b) RF loss *vs* CPW line thickness in µm

The previously studied CPW lines and TPV interconnects were fabricated using Au thicknesses below 1µm via lift-off [21], [45]. Electroplating allows for reaching higher thicknesses up to 5µm. Thicker Au is preferred for its stability and better RF performance. Also note that these RF transmission lines are fabricated in the same lithography step with final metallization pads for active PIC devices. So they also require good heat dissipation and good current injection uniformity into long active PIC devices [102], as discussed in Chapter 5 and 6. To find the optimal Au thickness in terms of RF performance, CPW lines were simulated using the 3D electromagnetic simulator CST studio. Figure 2.8.a) shows the graphic design system (GDS) design of CPW test structures containing the CPW line of variable lengths, GSG probe pad, and the transition in-between. The graded width of the transition maintains the impedance between the two structures. The ground, signal, and separation can be modified to

precisely tune the impedance to 50Ω [46], [103]. Similarly, TPV interconnects are designed with graded widths to maintain this impedance between the two interfaces, *i.e.*, lines on top of BCB and those at the substrate [45]. The transmission lines were optimized individually to maintain 50Ω impedance for several Au thicknesses. This was realized via an automatic optimization in the software, and the RF loss of the optimal configuration for each Au thickness is considered. Other relevant simulation details are found in [72]. Simulation results on RF losses of CPW lines on top of BCB *vs* Au thickness are shown in Figure 2.8.b). It can be seen that thicker Au results in lower RF losses because the skin effect is more prominent at thicknesses below 1µm [16].

Next, an experimental study was realized to characterize three CPW configurations having thicknesses of 200nm realized via lift-off, and 3-3.4µm realized via plating. These are, CPWs on top of BCB, CPWs on top of Si, and CPW lines on BCB and with GSG pads on Si, *i.e.*, containing two TPV interconnects. The last configuration is referred to as CPW+TPV. All configurations are shown in Figure 2.9.d). Dynamic electrical-electrical S-parameters of fabricated devices were measured using a 67 GHz VNA after standard short-open-load-thru (SOLT) calibration for de-embedding the setup's threaded cables and ground-signal-ground (GSG) probes, as discussed in [46]. The transmission losses per mm were then extracted based on raw S21 and S12 traces of CPWs with lengths of 100, 250 and 500 µm.

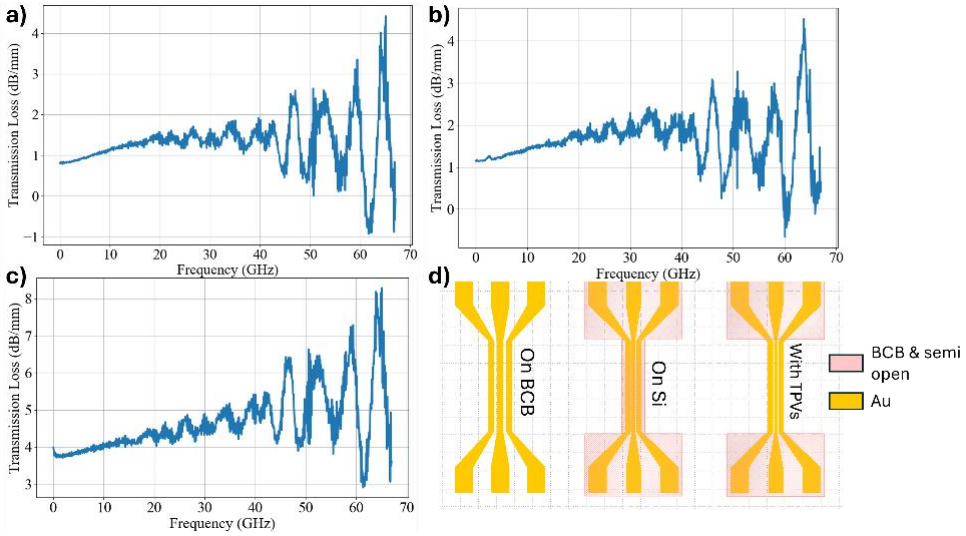

Figure 2.9 Transmission loss *vs* Frequency for CPWs with 200nm Au on: a) BCB, b) Si, c) CPWs on BCB and GSG pads on Si (CPW+TPV). d) GDS image of the structures

Results are shown in Figure 2.9 for the lift-off CPWs. The oscillation at higher frequencies is an artifact from the tool that was fixed in other measurements. The average RF losses at frequencies above 60GHz are around 2dB/mm for CPWs on BCB and Si while it increases to around 5dB/mm for the CPW+TPV structures. By comparing individual traces for these three structures at different length, an additional loss of 1.5 dB per TPV interconnect is incurred. This is mainly related to the high roughness of BCB that endured multiple etch backs during that run, and the fact that CPWs with thin Au are very sensitive to surface roughness [104].

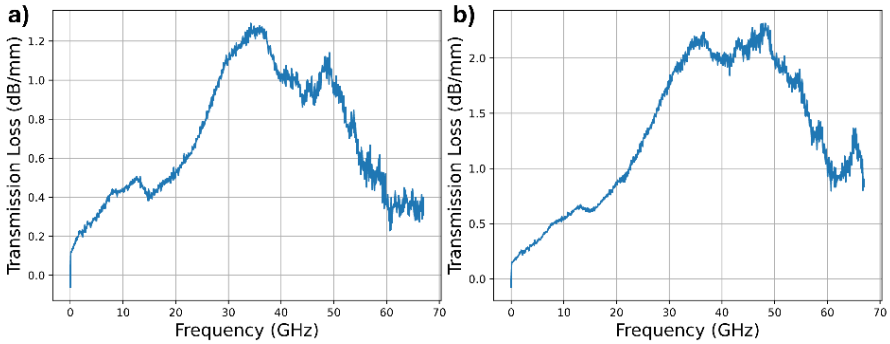

Figure 2.10 Transmission loss *vs* Frequency for CPWs with 3-3.4µm Au on: a) BCB, b) CPW+TPV

Results on 3-3.4µm-thick Au CPWs from the same wafer are shown in Figure 2.10. Here, CPWs on Si were not fabricated as a design mistake, so only those on BCB and CPW+TPV are measured. The maximum transmission losses for CPW lines on BCB is 1.2dB/mm for frequencies around 30-40GHz and it drops for higher frequencies. Similarly, the maximum losses of CPW+TPV are 2.3dB/mm for frequencies around 30-40GHz and it drops to 1dB/mm around 67GHz. By comparing individual traces for different structures at fixed lengths, the additional loss incurred by each TPV interconnect is around 0.5dB for frequencies between 30-50GHz and 0.4dB for frequencies around 67GHz. However, note that GSG pads de-embedding is more accurate to confirm this for all frequencies. For all of the measured devices with thick Au, the losses are highest between 30 and 50GHz. This might be related to the quality of the plated Au or an incomplete seed layer removal that leave Au traces. These fabrication issues might affect transmission at these frequencies. Also, note that the DC losses (frequencies close to 0GHz) are around 1dB/mm for CPWs with 200nm thin Au and 0.2dB/mm for CPWs with 3-3.4µm plated Au. This results from the higher resistance of thinner Au compared to the plated Au. The latter is also the lowest among CPWs fabricated from previous runs.

The characteristic impedance was also measured for all of these transmission lines. The measured impedance for all devices is around 15-25Ω higher than the designed impedance of 50Ω. This likely results from the high BCB roughness and lower conductivities of the deposited Au compared to the Au bulk properties used in simulations [72]. However, the impedance can be further tuned by increasing the signal width and decreasing the gap. Nonetheless, these studies show the potential of using thick CPW lines and TPV interconnects for 3D integration.

2.4.3 Optical considerations

In terms of optical considerations, all of the optical functionalities are realized within the photonic membrane with no partitioning. In principle, these devices can be flexibly placed wherever it is more convenient for the co-integrated layout to maximize their performance and minimize the interconnects length. This is also because membrane photonic devices benefit from full electric isolation, so they can be freely placed with no restrictions in terms of electrical crosstalk in-between. However, standard GCs used for I/O vertical coupling are affected by back reflections of light

coming from the substrate [105]. So these need to be placed in areas where there are no electronic devices on the bottom to avoid parasitic reflections. To retain this design freedom, GCs with back reflectors can be used. Here, the light is reflected by the thin layer of silver reflector that is 100nm beneath the membrane, and not from the EIC interface [106]. These also offer lower insertion losses and similar 3-dB bandwidths to standard GCs, but will require 2 extra post-bonding lithography steps. To mitigate fabrication risks, standard GCs are used in this work and special attention is paid to place them above blank areas in the EIC substrate, *i.e.*, containing only the SiO_2 and BCB after integration.

2.4.4 Thermal considerations

There are several challenges linked to thermal management of membrane PICs at different length scales [3]. These include heat extraction from hot spots for better energy efficiency, thermal conduction through the multi-layer stacks, different thermal properties and target temperature range for EIC and PIC devices, and thermal extraction from the SiP using active cooling elements [22]. For side-by-side integration used in optical communication systems requiring high spectral efficiency, the photonics require localized temperature control for stabilization, *i.e.*, cooling with a thermo-electric cooler (TEC). However, electronics can independently operate at higher temperatures (85+°C) with no required stabilization [41]. This operation mismatch presents a compromise between the energy penalty associated with cooling all components, or choosing localized cooling on PICs [41].

Similar to 3D EIC stacks, thermal managements of 3D E-PICs can be much more complex [7], [48]. This is because the goal of 3D integration is to achieve short interconnects and high density scaling capabilities, which can only be realized with multiple active PIC and EIC components (heat sources) vertically integrated and close to each other in a confined footprint [107]. So, the generated heat needs to be efficiently routed through components of the E-PIC device toward the package heatsink. This is to maximize heat extraction while efficiently controlling the thermal path for low thermal crosstalk between E-PIC devices. The goal is to preserve the device performance in the 3D stack relative to standalone devices at the two interfaces [94].

In terms of the co-integration technology presented in this thesis, these points are addressed with the following considerations. First, BCB has a relatively low thermal conductivity. So in Chapter 6, we discuss how to improve heat extraction from photonic devices using thermal shunts compatible with 3D integration and scalable in terms of density. Next, co-design rules need to be set based on the integration scheme and key device parameters to reduce thermal crosstalk.

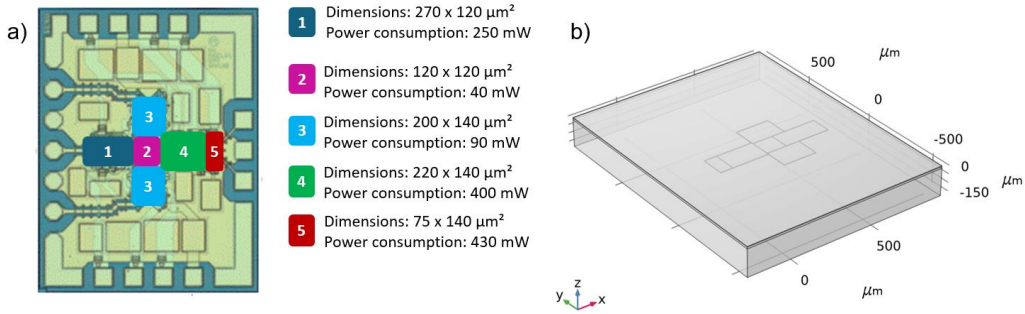

Figure 2.11 a) Simplified Tx IC power consumption, b) simulation setup matching the exact parameters of the circuit

Moreover, EICs generally consume higher power and generate more heat than PIC devices. So we assessed the thermal footprint of InP DHBT EICs to set the right co-design tolerances. Figure 2.11.a shows its geometry, containing around 100 DHBTs in 5 regions with different densities. The estimated power dissipation of each region is also shown. Figure 2.11.b shows the simulation setup to extract the thermal footprint. It consists of a 150 µm-thick InP substrate matching the chip thickness after thinning, and the 5 regions as 3 µm-thick InP blocks dissipating the indicated heating powers. For boundary conditions, a heatsinking temperature of 300K is set at the bottom of the InP substrate, while the top surfaces are set to natural convective cooling in air environment at room temperature with heat transfer coefficient h=5 W/m2/K. We compared the footprint before and after integration. For the former, the InP blocks contact the air, while for the latter the structures are embedded in thick BCB and topped by the InP membrane. The bonding BCB thickness was varied across a range of 4-20µm, while three InP membrane thicknesses were studied. These are 0.3µm,1µm and 2µm. Also, note that the top BCB interface represents the photonics and the bottom BCB interface represents the electronics.

The thermal footprint of an EIC topped by 10µm BCB and 2µm InP membrane is shown in Figure 2.12. It can be seen that most of the heat is concentrated in region 5, which represents the highest number and density of DHBTs among all regions. Figure 2.13.a shows the maximum top and bottom BCB interface temperatures for different BCB and membrane thicknesses. First, for the bottom BCB interface, the maximum temperature is stable over all simulation configurations and is within 1°C from bare EICs, *i.e.*, having no BCB+InP membrane on top. This is because the heat is mainly dissipated from the bottom of the InP substrate which is connected to the TEC, so the additional BCB and InP do not affect this heat dissipation. This is confirmed by comparing the performance of HBTs before and after depositing and locally opening 10µm BCB for stress tests, where the transition frequency dropped only by 5% (section 2.3.2). As for the top BCB interface, the temperature drops for increased BCB thicknesses, because BCB is highly insulating while the EIC hotspot is on the bottom interface with BCB. This drop is higher for thicker InP membrane thicknesses (Figure 2.13.a), because the latter helps in spreading the heat laterally through the membrane. Note that this only considers the effect of the EIC hotspot, and not active photonics when they are operating. For that case, higher BCB thicknesses trap more heat coming from the active photonics, as analyzed in Chapter 6.

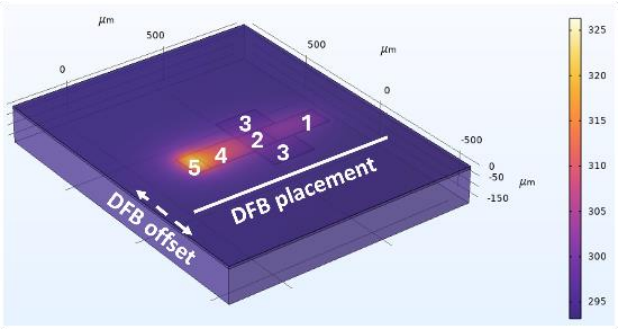

Figure 2.12 a) Tx IC thermal footprint at 10µm BCB and 2µm InP membrane thickness

Next, we assessed the thermal crosstalk between this EIC to a DFB on top for different DFB offsets. The offset is defined from the center of the hotspot to assess the impact of dense integration on DFB performance, as shown in Figure 2.12. The goal is to lower thermal gradients along the DFB length to below 10°C, to avoid affecting its performance while maintaining high integration density [10], [108]. The minimum and maximum temperatures across the full length of a 0.72mm DFB for different offsets are shown in Figure 2.13.b. A 0µm offset represents a DFB directly placed on top of the hot region in the EIC. Here, we observed that regardless of the BCB thickness in the range of 6-12µm, the difference between the maximum and minimum temperatures in the DFB can be lower than 10°C if the offset is higher than 100µm. So this is used as a co-design rule to ensure good DFB operation in the E-PIC. Finally, note that so far only bottom side cooling was considered, while simultaneous top side and bottom side cooling could be possible in the future, as described by the *IEEE roadmap* chapter 20 [3]. The latter could enable even lower crosstalk and higher density scaling.

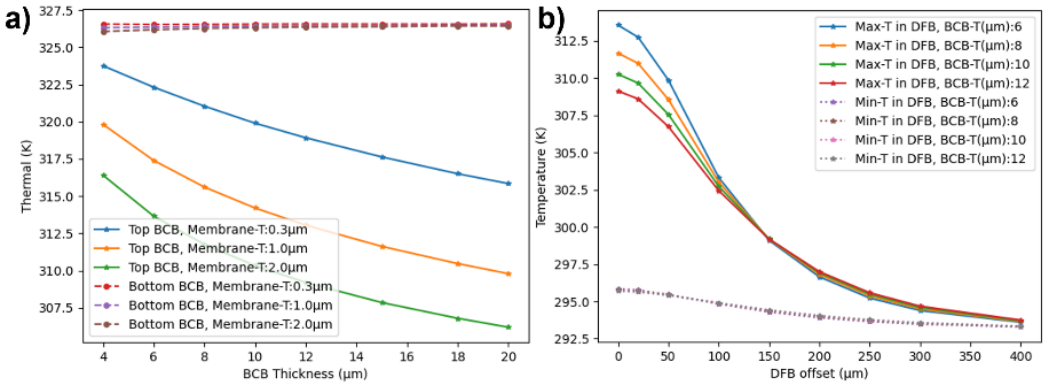

Figure 2.13 a) maximum top and bottom BCB interface temperatures *vs* different BCB and InP membrane thicknesses. b) maximum and minimum temperatures in the DFB region *vs* DFB offset for different BCB thicknesses

2.5 Conclusions

This chapter provided a comprehensive overview of the co-integration scheme and fabrication flow for InP-based E-PICs on the wafer scale. It addressed both technological

challenges and co-design considerations. First, the thermal tolerance of DHBTs was evaluated to define safe process boundaries. A process temperature cap of 240°C was defined to ensure that DHBTs performance remains uncompromised during bonding and post-bonding steps. EIC components were assessed for their compatibility with the co-integration process. Here, the post-bond processing temperature was capped at 240°C to avoid DHBT degradation, while the residual stress of BCB and SiO_2 used for bonding did not affect the performance of these devices. Protective coatings were also developed for the wet removal of the photonics wafer without damaging the electronics carrier. An optimal strategy consists of a 500nm pre-bond SiO_2, and thin ALD SiO_2 followed by a thicker SiO_2 and a resist coating on the backside of the electronics carrier.

Co-design rules were also set to enable functional 3D E-PICs. Key fabrication tolerances, such as a 15µm offset for BCB opening on EIC contact pads and post-bonding alignment compensation of up to 10µm, were established to ensure process reliability. Optical design freedom is retained within the photonic membrane while the I/O GCs can be placed near dicelines to avoid undesirable reflections. Electrically, RF losses as low as 1.2 dB/mm for CPW lines on BCB and an additional loss of only 0.4–0.5 dB per TPV interconnect at 67 GHz were demonstrated, highlighting their potential for high-speed and low-loss interconnects. Thermal management studies revealed the EIC driver hotspot regions, and that DFB lasers could be placed with only a 100µm offset to the high-power EIC regions to preserve its performance. These findings collectively demonstrate the feasibility of high-density, low-loss 3D co-integration, paving the way for scalable and efficient InP-based E-PIC solutions. Finally, the inherent process scalability to larger wafer sizes highlights its potential for high-volume manufacturing.

3

Chapter 3
A novel bonding process for 3D integration of InP membranes

This chapter presents a versatile method for improving post-bonding wafer alignment accuracy and BCB thickness uniformity in stacks bonded with soft-baked BCB. It is based on bonding with BCB micro-pillars that act as anchors during the reflow process. The anchor structures become a natural part of the bonding interface afterward, therefore causing minimal interference to the optical, electrical and mechanical properties of the bonded stack. We studied these properties for fixed anchor density and various anchor heights with respect to the adhesive BCB thickness. We demonstrated that the alignment accuracy can be improved by approximately an order of magnitude and approach the fundamental pre-bond alignment accuracy by the tool. We also demonstrated that this technique is effective for a large range of BCB thicknesses of 2-16 μm. Furthermore we observed that the thickness non-uniformities were reduced by a factor of 2-3 × for BCB thicknesses in the 8-16 μm range. [2]

3.1 Introduction

Wafer-scale bonding using adhesive polymers is an important processing step for multiple state-of-the-art microelectromechanical devices [109], PICs [16], [74], and in device packaging applications [110]. For photonics, adhesive bonding enabled heterogeneous integration of novel nano-photonic platforms offering high integration density, low energy consumption, and monolithic vertical co-integration with electronic devices [16], [68], [74]. The polymers used in this method, such as BCB, are compatible with most of the standard fabrication flows in terms of the thermal budget, material choice, and post-bonding processing. But to ensure a void-free bond with high post-bond mechanical strength and high tolerance to surface topography, low cross-

[2] This chapter is based on the work published in J9, C9, and P1.

linked (soft-baked) BCB is required [21], [110]. This is because the latter achieves low viscosity during bonding, hence wetting the bonding interfaces [110], [111]. BCB with higher cross-linking percentages turns into a gel-like state with no adaptability to surface topography. Thus, the bond can suffer from significant void formation and unbonded areas [111], [112]. However, bonding with soft-baked BCB results in degraded post-bonding alignment accuracy and BCB thickness uniformity. Moreover, the thickness of soft-baked BCB is required to be around 1.5-2 times the height of topographies in the two interfaces to result in void-free bonding, but higher thicknesses lead to larger degradation of these parameters [21].

High alignment accuracy is crucial for bonding applications where functional devices are vertically stacked, including vertical co-integration of photonics with electronics [16]. With state-of-the-art bonding tools, the attainable pre-bond accuracy is below 3 μm [113]. However, The post-bonding alignment accuracy with soft-baked BCB degrades quickly up to an order of magnitude higher for thicker BCB [21], [111], [113]. This is caused by the unavoidable presence of shear forces during bonding, acting significantly during the low viscosity state of BCB sandwiching the two substrates.

There are multiple ways to tackle post-bonding misalignment for soft-baked BCB. Using partially-cured BCB allows for better alignment accuracy but with no benefits of BCB reflow [112], leading to void formation for structured bonding interfaces [21]. Accounting for misalignment in the design layout results in larger devices and lowers the integration density and/or lower device performance. Further, Song *et al* [111] proposed to calculate the shift in misalignment using front-runners, and pre-compensating for it in the real identical wafers. But this requires running extra experiments if any processing condition is changed, and the method is not reliable for all material systems [21], [113]. Hence, processes that directly block misalignment are preferred. For instance, mechanical anchors can be fabricated to join the two wafers together during bonding and hence limit misalignment [110]. Aluminum-based anchors were tested for 2-μm thick BCB and provided good anchorage with lower misalignment [113]. Interlocking anchors were also investigated for various systems and 0.2-μm thick BCB [114], [115]. However, asides from the bond-quality issues, both methods were only tested for < 1 μm-thick BCB. They are also difficult to be integrated in mature process flows because of the complex fabrication and possible incompatibilities with standard flows. For instance, compatibility checks are needed before depositing and patterning thick metals or semiconductors for anchors on semi-processed wafers. Moreover, using interlocking anchors for bonding substrates with different CTEs is not possible, as the substrates would expand and retract at a different rate during bonding. These methods also increase dead space where no device or fabrication test structures can be placed.

Another compromise of soft-baked BCB is the significant post-bonding thickness non-uniformity [93]. Good thickness uniformity after bonding is important in multiple aspects. First, if post-bonding processing requires etching of the adhesive film to fabricate TPVs for instance, it becomes complicated to open all areas at the same time when the film is highly non-uniform. Secondly, thickness variations can directly affect device performance. Moreover, for IMOS active devices [68], the heat is mainly dissipated through the Si carrier wafer. Higher thicknesses yield lower heat dissipation and therefore degraded performance [21]. Also, photonic devices such as phase shifters require good heat isolation, so these can be impacted if Al-based anchors are used as the additional metal provides a thermal path to the substrate. For GCs, variations in the

bonding thickness yield variation in the coupling efficiency depending on the interference [105]. Therefore, high thickness non-uniformities lead to unpredictable and possibly degraded device performance. To our knowledge, there are no current methods that tackle this issue for bonding with soft-baked BCB.

In this chapter, we investigated the possibility to use wafer-scale uniformly distributed BCB-based anchors to improve the post-bonding alignment accuracy and BCB thickness uniformity. The BCB anchors are fully crosslinked, serving as solid anchor structures. Unlike other anchor methods, the proposed method offers minimal change to the optical, electrical and mechanical properties of the bonding interface, because the anchors and the bonding layer are based on the same material. As a result, the method achieves a uniform bonding layer and does not introduce dead space nor influence post-bonding processing. It could also be applied to other polymers used in adhesive bonding if the anchors are dense and have sufficient mechanical strength to serve their intended purpose. Here, we fixed the density of anchors (fill ratio) at 20% and systematically studied the effect of adding the anchors to the bonding process for BCB thicknesses in the 2-16 μm range. The physical characteristics of the anchors and important parameters for post-bonding processing were also investigated.

3.2 Concept and fabrication

In this study, we chose to bond wafers of the same material, *i.e.,* no CTE mismatch to avoid having post-bonding geometric distortions and misalignment due to expansion, hence making sure the obtained misalignment is attributed to substrate shifts alone [114], [116]. Moreover, given that misalignments from expansion need to be corrected in the mask layout in any case, this method can be applied to heterogeneous substrates as well. Therefore, we used glass-glass wafers with markers to study the alignment accuracy, as their transparency helps in verifying the pre-bond alignment and facilitates characterization. We also used bare InP-InP wafers to study the thickness uniformity, since reflectometry was used for accurate thickness mapping after removing the top wafer. Details of all experiments are listed in the two following results sections to avoid redundancy (Table 3.1 and Table 3.2). The general process flow we followed to fabricate the wafers and bond them is shown in Figure 3.1.a). An illustration of the pre- and post-bonding wafer stacks are shown in Figure 3.1.b) and .c), respectively.

For the glass wafers, we used 3-inch double-side polished Fused Silica Wafers with a bow of < 20 μm and thickness of 500 μm. For the InP wafers, we used test-grade wafers with bows of < 30 μm and thickness of 650 μm. The bows of each wafer were measured using profilometry and matched such that wafers 1 and 2 (Figure 3.1) have a similar bow profile and values. The latter is realized to avoid having a high bow mismatch that can potentially introduce post-bonding residual stresses and thickness variations, which can introduce additional errors in our results [117]. As a result, the bow of the bonded stack is minimized.

We start the fabrication by pre-cleaning the substrates in O_2 plasma. Next for the glass wafers, we deposit and pattern 10/100 nm-thick Ti/Au alignment markers via lift-off. The pattern consists of 12 alignment keys distributed along 2 rows in the wafer. Subsequently, we deposit and outgas 500-nm thick SiO_2 layer, and spin-coat a layer of AP3000 to optimize the adhesion of BCB to the wafers.

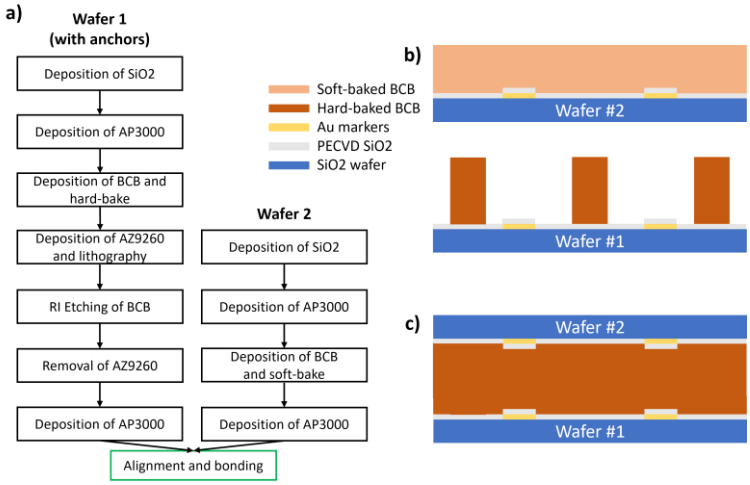

Figure 3.1 a). Fabrication process flow of the full bonding stack. Illustration of the bonding stack using BCB anchors: b). Pre-bonding, c). Post-bonding

We studied BCB thicknesses of 2, 4, 8, and 16 µm, so we used Cyclotene 3022 -46, -57, and -63 at different RPMs to achieve these target thicknesses with optimal uniformity after spin-coating. For wafer 2 (Figure 3.1.a), the BCB is then soft-baked at 100 °C for 5 min, and an extra layer of AP3000 is applied to improve adhesion of BCB to the BCB anchors during bonding. This is referred to as bond BCB. To fabricate anchors on wafer 1, we used the same BCB as on wafer 2 to investigate the variation in physical properties between the two. After BCB deposition and soft-bake, we hard-bake the stack in an N_2 environment at 280 °C for 1 hr to ensure full-crosslinking of BCB inside anchors. Next, we spin-coat 25-µm thick AZ9260 resist and pattern it via photolithography, then we subsequently transfer the pattern to BCB with O_2:CHF_3 5:1 plasma RIE etching and reapply a final layer of AP3000. It is important to note that a 12% reduction in height is obtained after hard-baking BCB, therefore, the anchors in wafer#2 are 12% shorter than the thickness of the soft-baked BCB in wafer#1 before bonding.

To bond the wafers, we first align them in a commercial EVG aligner using the crosshair method, whereby the markers of wafer 2 are located and the crosshairs of these markers are registered in the system, the markers of wafer 1 are then aligned to these crosshairs. Next, the wafers are brought into contact, and we visually inspect the alignment and then lock the stack in a cassette holder. This procedure allows us to achieve 1-2 µm accuracy. The cassette is then loaded into the EVG bonder. Bonding is realized in vacuum (<10^{-5} Torr) where the stack is heated at a rate of 5 °C/min while applying a force of 700N, the force is then released and a full-cure of 1hr at 280 °C is realized. For the InP stacks after bonding, wafer 2 is selectively etched in HCl:H_2O 4:1 at 35°C to reveal the adhesive layer. A dielectric multi-layer is deposited on the backside of wafer 1 before etching to protect it.

This seamless fabrication of anchors means they can be put anywhere in the wafer. Therefore for the mask layout, we chose a real layout used in the co-integration of PICs with electronics. The mask layout consists of different 5×5 mm^2 reticles repeated throughout the wafer. The average size of these rectangular anchors inside each reticle

is around 0.1 ×0.1 mm² and the minimum spacing between anchors is ≈10 µm. Also, given that shear forces present during bonding are low compared to compression forces [111], a fill factor, *i.e.*, the density of anchors relative to empty space, of ≈1 % was enough to block misalignment using Al-based anchors [113]. In our case, the hardness of BCB is ≈20x lower than Al sputtered thin films [118], [119]. Considering that these anchors do not increase dead space, we fixed the density to 20 % for all of our experiments using BCB anchors.

After fabrication, all stacks are inspected using optical microscopy to calculate the misalignment and assess void formation, SEM to inspect the interface between BCB film and BCB anchors, and reflectometry with profilometry for thickness measurements. We also used NIR ellipsometry to extract the optical properties of BCB. For that, we fitted the results using the Cauchy model with a mean square error <50 [120]. For reflectometry, each map was obtained with 65 points evenly distributed across the 3" wafer, and we used 3 mm edge exclusion in all maps.

3.3 Improvement of the alignment accuracy

For BCB bonding of wafers with identical CTE, misalignment errors mainly result from shifts (translations) in the (x,y) plane, where x is the direction perpendicular to the wafer flat. Rotations are minimized in state-of-the-art tools, and orthogonal and non-orthogonal expansions only result from CTE mismatch between the bonded wafers [93]. The designed role of anchors is to provide solid mechanical support between the two wafers during bonding, and thereby limit the misalignment. Therefore, misalignment due to rotation might also be suppressed using this method, if present.

Table 3.1 Wafer-scale misalignment of all glass-glass bonding experiments

Exp N	BCB thickness (µm)	Anchors thickness (µm)	average shift in x-direction (µm)	average shift in y-direction (µm)	total misalignment (µm)
1	2	0	4.6	29.5	29.9
2	2	0	1.0	32.6	32.6
3	2	2	2.8	1.7	3.3
4	2	2	1.2	0.5	1.3
5	8	0	36.5	1.5	36.5
6	8	0	58.0	12.0	59.2
7	8	0	13.0	8.0	15.3
8	8	4	1.6	15.6	15.7
9	8	4	6.6	6.1	9.0
10	8	8	6.2	4.6	7.7
11	8	8	3.2	2.2	3.9
12	16	0	137.0	47.0	144.8
13	16	0	40.0	18.0	43.9
14	16	16	7.8	1.1	7.9
15	16	16	3.0	2.0	3.6

Results on the wafer-scale shifts of all experiments are listed in Table 3.1. Here, we considered the average shift of all 12 alignment keys since the variation between

individual values is small given the identical CTE between wafers and negligeable post-bonding rotation. Moreover, the anchors are supposed to block shifts regardless of the direction, which is why we simplify our analysis by using the total misalignment. Results are plotted in Figure 3.2.a for stacks without *vs* with anchors having matching heights to the bonding thickness. We also included the average values of alignment keys from [121] given that similar bonding parameters with soft-baked BCB were used. For Figure 3.2.b, we plot misalignment *vs* height ratio of anchors for bond BCB thickness of 8 µm.

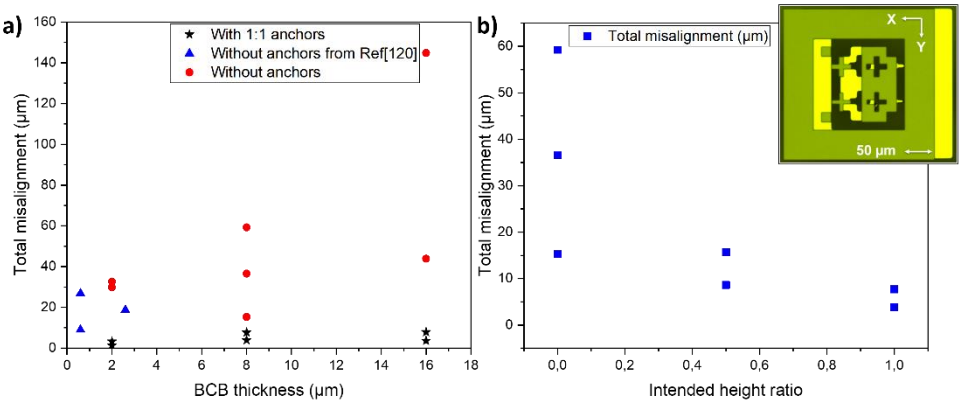

Figure 3.2 Total misalignment of bonded glass stacks with and without 1:1 height ratio anchors *vs* BCB thickness. b). Total misalignment of bonded glass stacks with 8µm bond BCB *vs* anchors height ratio. Inset: microscope image of misaligned markers N5.

Starting with bonded stacks without anchors, the wafer-scale total misalignment increases significantly with increasing BCB thickness (Figure 3.2.a), This is because soft-baked BCB reflows during the bonding, and thereby serves as a lubricant with higher viscoelasticity for higher thicknesses, allowing one wafer to shift from the original position with respect to the other [110]. This wafer-scale shift is attributed to the presence of shear forces during the reflow state of BCB [111]. We also note that the shift values in x-direction are higher than in the y-direction for 8- and 16-µm BCB, and *vice versa* for 2-µm BCB, which signifies an interplay between a preferred directionality (systematic shift) and non-directionality that are affected by BCB thickness.

In our bonding process, this systematic shift is likely caused by an uneven clamping force of the cassette holder, since the clamping force was intentionally lowered to avoid cracking of the fragile InP wafers, and the x-direction is on the same axis of the two pins in the holder. It is worthwhile to note that these EVG bonder and bond aligner imperfections fall within its fabrication tolerances and cannot be improved. A consistent wafer-scale systematic shift was expected for similar bonding conditions depending on the value of shear forces and viscosity of BCB [111]. However, high variance was recorded in our results and also from Niklaus [112], [113]. This variance is attributed to inhomogeneities in the BCB reflow process during the bonding caused by non-uniform compression [121]. Indeed, the thickness variation stays high as the BCB thickness increases, as discussed in the next section, and the absolute thickness variations also further diverges for higher BCB thicknesses leading to high variance. Moreover, wafer bow and shear force non-uniformities caused by the total thickness

variation (TTV) of the wafers might also contribute to this variance [111], [117]. This variance might also be exacerbated by the presence of particles at the bonding interface, since particles with larger dimensions than the bonding thickness would force the reflow of BCB to accommodate its presence depending on the compression force it can handle. Therefore, uneven distribution and concentration of sandwiched particles can contribute to variations in the random shift between samples. However, the effect of particles presence does not explain the increase in variance when the thickness increases. Investigating the variance itself is indeed cumbersome as it would require repeating the experiment multiple times to gather enough, which is outside the scope of this study.

For the bonded stacks having anchors with the same height as the bond BCB (Figure 3.2.a), the wafer-scale misalignments after bonding are lower than 10 µm for 8- and 16-µm BCB and < 5 µm for 2-µm BCB. These results are comparable to anchors fabricated with Aluminum along the edge of the wafer [113]. In both cases, the presence of anchors between the two wafers suppresses the shift to a good extent. Moreover, both systematic and non-systematic shifts are suppressed to a good extent (Table 3.1) whereas the variance in misalignment between samples is also comparably high, signifying that the anchors do not fully suppress one mechanism above the other. Moreover, the variance does not significantly increase when the thickness is varied from 2 to 16 µm highlighting that the anchorage works in a similar manner for all thicknesses. This alignment tolerance is compatible with the 3D co-integration flow discussed in Chapter 2.

As will be discussed in the next section on the thickness variation suppression using anchors, the existence of thickness variation with samples having anchors can be the reason for the incomplete suppression of the shift with the anchors. This is because regions with low pressure during bonding would have a higher thickness than the intended thickness, and thereby anchors in these regions do not reach the other substrate, hence these anchors would not function. This implies that the effective density of working anchors is reduced because of thickness variations. To investigate this, we varied the height of anchors relative to a bond BCB thickness fixed at 8 µm. Results are shown in Figure 3.2.b, where the ratio represents the height of the anchors relative to the bond BCB. Indeed, we see that both misalignment and variance in misalignment increases for bonding experiments with anchors having a height ratio of 0.5 compared to 1.

Finally, the introduced BCB-based anchors added frictional forces between the two substrate surfaces that acted against the shear forces during the liquid state of BCB, resulting in lower misalignment. This mechanism can therefore be extended to inhibit wafer shifts being the main or a component of the total misalignment in other systems that involve BCB bonding, such as bonding InP to InP or InP to Si.

3.4 Improvement of the bond uniformity

An image of the BCB fringe pattern and reflectometry map of samples from Exp N.20 and N.22 (Table 3.2) are shown in Figure 3.3. The reflectometry maps are analyzed and results are summarized in Table 3.2. Asides from experiments on soft-baked BCB, we also fabricated and analyzed 2 reference samples. In Exp N.16 we measure a fully cured BCB after spin-coating, and in Exp N.17 we used 8-µm thick BCB layer that was partially cured at 175 °C for 1hr to bond InP-InP stack with the same bonding parameters as

before. The goal was to assess the thickness non-uniformity for bonding using partially-cured BCB, which we expect to be better than soft-baked BCB [112].

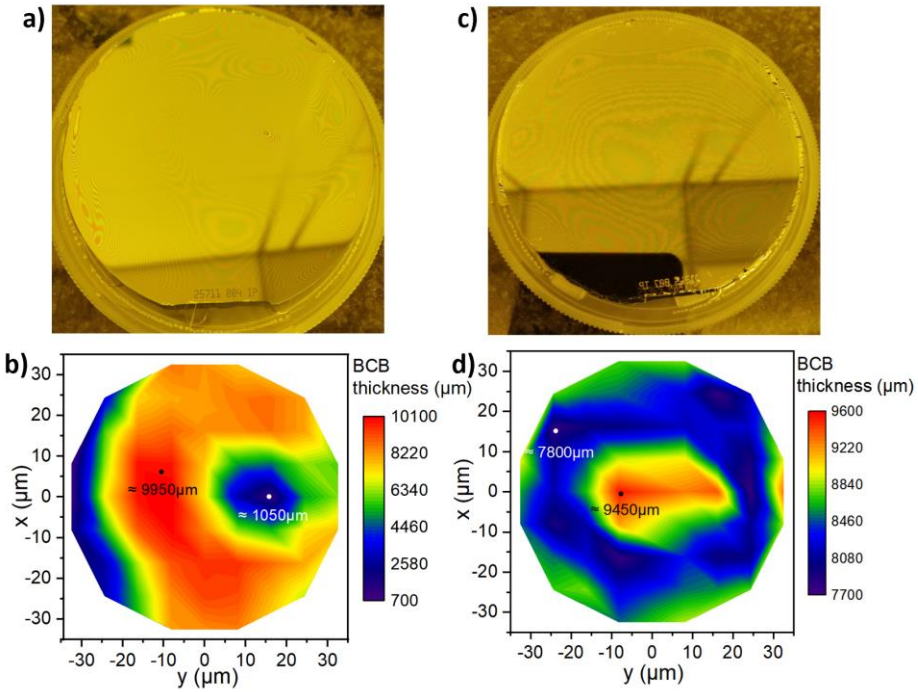

Figure 3.3 a). BCB pattern of a bonded stack without anchors (Exp 20), and b). its corresponding reflectometry map. c) BCB pattern of a bonded stack with 1:1 anchors (Exp 22), and d). its corresponding reflectometry map.

As seen in Figure 3.3.a) compared to 3.c), the wafer-scale BCB fringes are denser, which signify higher thickness variations when anchors are not employed. Moreover, the locations with min and max thicknesses are randomly distributed along the wafer without preferred location in most of the samples. This might be related to the presence of randomly placed particles with higher dimensions that force redistribution of the liquid BCB, or non-uniform presence of residual forces, for instance during clamping of the cassette while alignment or because of the TTV of the wafers.

Looking at results from Table 3.2, the thickness variation for the hard-baked BCB reference is only 1.3 % since high uniformity is expected after spin-coating. This uniformity also translates to high uniformity in the thickness of anchors used for subsequent bonding. The thickness variation in the partially cured reference is 9.6 % however. This is because the bonded area in this experiment is ≈ 80% of the total wafer thickness, due to the existence of a BCB edge bead of 15-µm that inhibits bonding the full area without applying higher force. The thickness variation range of samples without anchors is ≈90-120% and ≈75-120%, for 8- and 16- µm BCB, respectively. This is caused by the reflow of BCB during bonding, which allows it to be expelled from high compression points and accumulate near low compression regions in the wafer. The source of this variation might be attributed to multiple reasons, like using test-grade wafers having small defects, different matched bows, residual stresses after clamping

the wafer, etc. However, the goal here was to test the improvement using BCB anchors and not optimize the uniformity.

Table 3.2 BCB post-bonding thickness variations obtained from reflectometry. Exp N.16 (highlighted in gray) represents a Hard-baked BCB reference without bonding. Exp N.17 (highlighted in blue) represents a reference stack bonded using partially baked BCB at 175 °C

Exp N	BCB thickness (µm)	BCB anchors height (µm)	Lowest thickness (nm)	Highest thickness (nm)	Average thickness (nm)	Variation (%)	Standard Deviation (nm)
16	8	0	8499	8615	8545	1.4	28
17	8	0	7786	8562	8050	9.6	150
18	8	0	4431	10971	7219	90.6	2411
19	8	0	3833	11096	8510	85.3	1604
20	8	0	712	10079	7644	122.5	1938
21	8	8	7736	9545	8514	21.2	528
22	8	8	6999	10161	8508	37.2	973
23	8	8	7079	11009	8510	46.2	979
24	16	0	3271	20216	14463	117.2	3841
25	16	0	7961	18162	13574	75.2	2938
26	16	16	15483	22523	17671	39.8	1482

The range of non-uniformity is reduced to ≈21-46% and 40% for 8 and 16 µm BCB thicknesses, respectively, for samples with anchors matching the height of the BCB thickness (height ratio 1). Moreover, because of local thickness variations, some regions have a higher thickness compared to the intended thickness, and hence a lower percentage of anchors reaches the other substrate. Although it is difficult to pinpoint the exact value for this *effective* density, the designed density of 20 % was sufficient in reducing the thickness non-uniformities.

Moreover, the average BCB thickness for samples without anchors is higher than that with anchors for the studied thicknesses. We suspect that the volume occupied by anchors (20 %) is not fully dissipated from the bond BCB during the short time when BCB is liquid such that the measured average post-bonding thickness is higher than the intended value. This could be due to the lower bonding pressure applied to avoid breaking wafers. Hence we note that the fill ratio of anchors needs to be accounted for in choosing a lower corresponding thickness of bond BCB for optimal anchoring. The correct thickness might depend on multiple parameters such as the fill factor of anchors, applied bonding force, temperature ramp-up speed, etc.

Given the randomness of thickness max and min points (Figure 3.3.b and Figure 3.3.d), an optimal performance of anchors can be achieved with a uniform distribution of anchors along the wafer rather than having anchor concentrated only in specific locations, for example at the wafer edges [113]. This ensures that the anchors block redistribution of BCB from high to low compression points.

3.5 Physical and mechanical properties of the bond layer

Figure 3.4.a) shows an SEM picture of anchors before bonding and Figure 3.4.b) shows a cross-sectional picture of the anchors after bonding near the anchor-BCB interface. A sidewall angle of 37° is distinctive at the interface (Chapter 2). It can be seen that the interface is perfectly continuous without introduction of voids. The dark line at the interface is apparent because of electric charging during the long exposure to acquire the image. Here, BCB reflows well to cover the areas between anchors without leaving voids. Also, given the high thickness non-uniformity, in some images the top of the anchor does not fully reach the other surface. Moreover, we RIE etched 2-µm deep into BCB to reveal the interface between the anchors and bond BCB, an angled top-view SEM image of this interface is shown in Figure 3.4.c). Here, the interface between anchors and the bond BCB (highlighted in red) is not interrupted by any void. The surface pattern inside anchors is denser compared to the bond BCB, which is related to the different thermal treatment history of BCB inside anchors and the bond BCB. This is believed to be caused by the vitrification of BCB whereby the free volume of BCB is decreased, and hence a denser etch pattern is obtained [122].

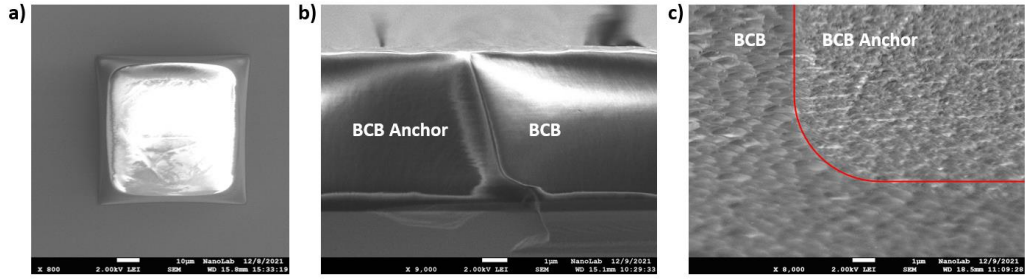

Figure 3.4 a). Top view of a standalone BCB anchor before bonding. Post-bonding interface between 8-µm BCB and 8-µm BCB anchors (Exp N:21: b). cross-sectional view c). Angled top-view after uniformly etching 2-µm deep into BCB

Furthermore, we assessed the optical properties of anchors relative to the bond BCB to determine if they can be placed near photonic devices. For this, NIR ellipsometry measurements were carried out on reference samples. The samples consisted of 1-µm thick BCB treated at 280 °C for 1hr and 2hrs, and at 250 °C for 1hr and 2hrs. The latter was additionally investigated given that full curing can be achieved at that thermal budget [121]. We chose this thickness to obtain the highest fit possible given that our interest lies in the refractive index difference. Results are shown in Figure 3.5. The measured refractive index difference for samples treated at 250 °C is below 0.025 over the full wavelength range, whereas the variation for samples treated at 280 °C decreases steeply from 0.08 at 300 nm to 0.025 at 600 nm and stabilizes below this value at higher wavelengths. This is largely because of the higher shrinkage of BCB when cured at a higher thermal budget (time and temperature) [112], [122]. The fitted thicknesses are 1080±2.5 and 1073 ±2.5, 1047±3 and 994±3 for samples treated at 250 °C for 1 and 2 hrs, and 280 °C for 1 and 2 hrs, respectively. So the difference in thickness is 7±5nm and 53 ±6 nm for samples treated at 250 °C and 280 °C respectively, which support the higher condensation at higher thermal budgets.

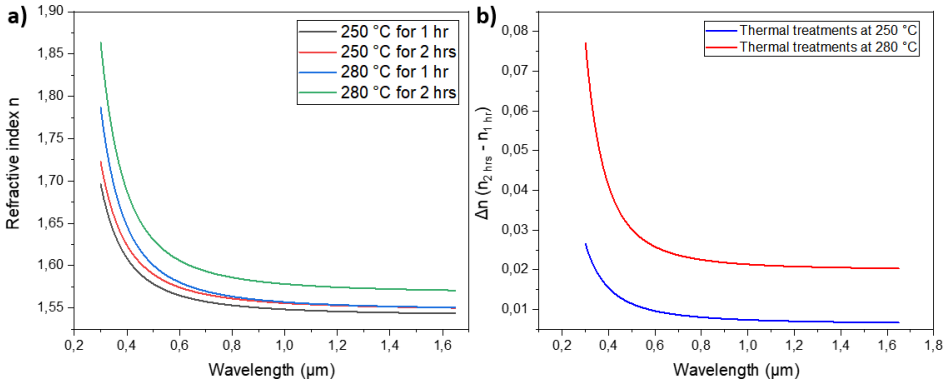

Figure 3.5 a) Refractive index of BCB treated at different conditions. b) Refractive index difference for BCB treated at different times and fixed temperature

One crucial post-bonding processing step for co-integration of photonics with electronics is BCB etching [16]. We used the reference samples previously discussed to determine the etch rate difference between samples treated at different thermal budgets. We found that the etch rate difference is below 3% for samples treated for 1 hr and 2hr at 250 °C and 5% for samples treated for 1hr and 2hr at 280 °C. This slight variation in etch rates is related to the higher density of BCB treated at higher thermal budgets [122]. These variations are much smaller than the variations in BCB non-uniformities after bonding that need to be accommodated for during BCB etching to create TPVs. Therefore, no optimizations of post-processing steps are required and the design of anchors in terms of shape and distribution is not constrained.

Furthermore, for the mechanical properties, we evaluated the residual stress of anchors and BCB used for bonding. This is because a high-stress difference could result in the partial detachment of anchors from the bond BCB, leading to void formation at the interface. This is especially important if the anchors are close to or embedding devices, for instance if the chip layout does not offer blank space for anchors. The residual stress of BCB *vs* baking temperatures was previously studied for 2.5 µm BCB [123]. However, a comprehensive study on the effect of BCB thickness and cure time is required to fully encompass the process parameters varied in our study. Here, the anchors are cured for 1h at 280 °C, and the bonding is carried out in the same conditions afterward. Hence, we fixed the temperature at 280 °C and cured BCB for 1h and 2h to investigate the stress difference. The studied BCB thicknesses are 1, 4, 8, and 16 µm. The thickness uniformity is above 95% after cure, therefore the effect of thickness non-uniformity on stress is negligible. The process flow consists of depositing and baking BCB on 3" Si and InP substrates for reproducibility. The wafer bow parallel and perpendicular to the major flat is tracked before BCB deposition and at each step of thermal treatment. The stress is then extracted from bow values using Stoney's formula given below [124].

$$\sigma = \frac{E_s}{6(1-v_s)}\frac{h_s^2}{h_f^2}\left(\frac{1}{R}-\frac{1}{R_s}\right) \qquad (1)$$

Here, E_s and v_s are the Young modulus and Poisson ratio of the substrate, h_s and h_f are the thicknesses of the substrate and deposited thin film, and R_s and R are the substrate curvature radius before and after deposition (or thermal treatment in some cases of this study). The bow profiles are measured using profilometry and fitted to extract accurate bow values. The process flow starts with cleaning the wafers and depositing and outgassing 50 nm SiO_2. BCB is then deposited and cured for different periods. The bows are tracked between each deposition or curing step. The BCB thickness is tracked with reflectometry. The average bow is plotted for each thickness and curing time for Si and InP carriers in Figure 3.6. Moreover, the stress expected from CTE mismatch between BCB and the carrier wafer is given by:

$$\sigma = \left(\frac{E_{BCB}}{1 - v_{BCB}}\right)(\alpha_{BCB} - \alpha_{carrier})\Delta T \qquad (2)$$

Where E_{BCB} and v_{BCB} are the Young's modulus and Poisson ratio of BCB, α_{BCB} and $\alpha_{carrier}$ are the coefficients of thermal expansion of BCB and the carrier wafer, and ΔT is the temperature treatment window. Results show that the residual stress is tensile-strained, because of the higher stretching and contracting of BCB. The theoretical BCB residual stress treated at 280°C is 67.5 MPa for BCB on Si and 65.2 MPa for BCB on InP. However, the experimental values are between 36-48 MPa for all BCB thicknesses. This results from the partial relaxation of BCB stresses given the mobility of polymer chains at this temperature [123]. The stress difference for BCB treated at 1h and 2h is below 2 MPa for all measurements, confirming that a bonding interface consisting of BCB anchors and BCB bond layer is continuous and almost uniform in terms of stress. The difference is low because the residual stress of BCB is mainly dominated by the difference in CTE between BCB and the used substrate at a given temperature [123]. Moreover, since BCB has CTE at least an order of magnitude higher than that of most solid-state substrates [125], the residual stress is mainly dominated by the BCB being a polymer, and stress values are similar for different substrates (Figure 3.6). Therefore, we identify a low risk of stress-induced detachment at the interface as confirmed by SEM imaging (Figure 3.4.b), and this likely extends to most of the other solid-state substrates as well.

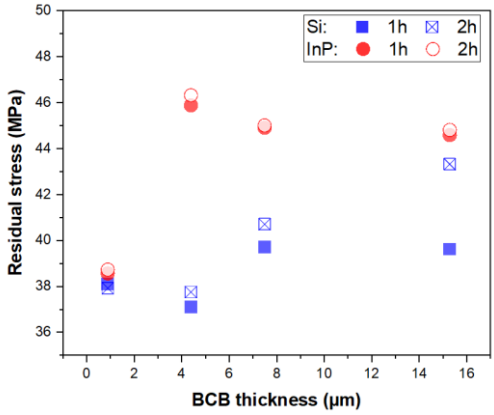

Figure 3.6 Residual stress of BCB deposited on InP and Si and treated at 280 °C for 1h and 2h.

For further improvements to achieve anchors with matching optical properties to the bond BCB, optimizing the thermal budget to maintain good mechanical properties of anchors and close physical properties relative to the bond BCB might be an option. By good mechanical properties we refer to high hardness and Young's modulus for the anchors so that they sustain higher compression pressure without plastically deforming. For the choice of thermal budget for anchors, other factors can also be included in this choice such as higher adhesion between anchors and the bond BCB. In fact, instead of ≈100 % crosslinking, it could be better to choose lower cross-linking percentages to better match the thermal budget with the bond BCB. For BCB, the optimal crosslinking percentage of anchors is at 85-90% instead of 100 %. This can lead to an improvement in adhesion to bond BCB by a factor of 3-4 [126] while the hardness stays relatively the same and Young's modulus only reduces by ≈1.2-1.5× [118]. Finally, we demonstrated improved post-bonding alignment accuracy and bond uniformity with a fixed anchor fill factor of 20%. The fill factor can be further investigated to find the boundaries of this method.

3.6 Improvement of the alignment with processed wafers

To investigate the effect of BCB anchors on post-bonding properties of processed InP wafers, we performed three InP-InP bonding experiments with backside alignment, as described in the previous chapter. The first is a reference bond with no anchors, labeled as sample 1, whereas the second (sample 2) and third (sample 3) experiments do contain anchors. The difference between sample 2 and 3 is whether they contain surface topology (resulting from processing) or not. Table 3.3 summarizes these details. A schematic illustration of the InP-InP alignment bonding for sample 3 is similar to Figure 3.1, except the addition of backside markers. Similar to Figure 3.1, wafer #1 and #2 contain topologies similar to those present in real wafers used for 3D integration. The targeted BCB thickness is 10-12 µm for co-integration as discussed in the previous chapter. For sample 2, wafer #2 has no topology except for the Ti/Au markers with a thickness of about 100 nm. As for sample #3, wafer #1 and #2 are actually test wafers intended for co-integration process development (chapter 2), from which, wafer #2 was provided by III-V lab and contains 3 µm of topology, similar to the actual electronics wafer.

Table 3.3 Summary of InP-InP alignment bonding tests

Sample N	Bond layer BCB thickness (µm)	BCB anchors height (µm)	InP topology (µm)	Misalign-ment in x (µm)	Misalign-ment in y (µm)
1	10	0	0	24.6	5.3
2	10	10	0	8.2	4.2
3	10	10	3	7.3	5.8

Bonding was realized according to optimal conditions for co-integration discussed in the previous chapter. After bonding and removal of one of the substrates, the wafer-

scale average misalignments are shown in Table 3.3. These values take into account the fundamental alignment inaccuracies from the bonder tool during backside marker fabrication and wafers alignment for bonding, which are both in the order of 1-2µm [19]. Hence, the misalignment decreases by at least 15 µm to values below 10µm with the addition of anchors for this BCB thickness, *i.e.*, >150% improvement. This is sufficient for co-integration since the pad areas are typically in the order of 50-100µm in size. Moreover, compared with sample 2, the introduced topology in wafer#2 for sample3 did not affect the misalignment values, which guarantees the feasibility of this process for real co-integration. Also, these values are similar to the experiments performed by bonding glass to glass at higher ramp up rate of 10°C/min as shown previously, which signifies that the method can be used for a wide range of materials.

3.7 Conclusions

In this chapter, we used BCB-based anchors to improve the post-bonding thickness uniformity and alignment accuracy for a wide range of BCB thicknesses. By using BCB anchors, the alignment accuracy has improved by an order of magnitude and approached the fundamental pre-bond alignment accuracy of the tool for BCB thicknesses in the 2-16 µm range. And the thickness uniformity improved by a factor of 2-3x for BCB thicknesses in the 8-16 µm range. We also highlighted the importance of matching the height of anchors to the BCB thickness used for bonding for better alignment accuracy. The process was also verified for patterned wafers with topology. Finally, an added advantage to using the same BCB for anchors and adhesive bonding is the similar physical and mechanical properties between the two after bonding and seamless fabrication of anchors.

4

Chapter 4
Mapping and analysis of spatial distortions in InP membranes

Heterogeneous integration helps to maximize the performance of SiPs by leveraging the strengths of diverse material platforms within a unified process flow. A promising approach is the 3D integration of InP photonic or electronic membranes to other substrate materials containing photonics or electronics ICs via adhesive bonding. However, wafer-scale spatial distortions arising from the bonding process can compromise fabrication. Herein, we used electron-beam metrology to investigate the distortion of InP membranes resulting from wafer-scale bonding with BCB. We measured both the linear and residual components of distortions across the tested wafers. First, bonding of InP substrate with BCB on various carrier substrates (Si, InP, SiC, and glass) was realized, which unveiled post-bonding membrane expansion factors in the range of ~0-325 ppm and beyond that for the glass carrier. The divergence of these values from theoretical estimations was linked to the adhesive bonding process. Next, we examined the effect of BCB thickness in the ranges of 1-12μm, residual mechanical stress, and the impact of defects on distortions. Using these findings, we experimentally verify that the largest part of distortions can be effectively pre-compensated to overcome the challenges of multilayer overlay errors in the fabrication of heterogeneously integrated photonic and electronic devices. [3]

4.1 Introduction

Photonic integration is a rapidly evolving field, which has the potential to revolutionize a multitude of applications, ranging from telecommunications to quantum computing.

[3] This chapter is based on the work published in J6 and C8. For contributions, Aleksandr Zozulia (PhI group, TU/e) helped in fabrication and discussions. Jeroen Bolk and Erik Jan Geluk (NanoLab, TU/e) helped in discussions.

In the past years, multiple material platforms were introduced for the fabrication of photonic integrated circuits, such as SiPh, InP photonics, SiN photonics, etc. Each of them has their key advantages in a specific range of applications. A growing trend is heterogeneous integration, which harnesses the best features of different platforms and unites devices from different materials in a single assembly on a chip scale or full wafer scale. The scope of heterogeneous integration covers a wide range of applications, including ultra-low linewidth lasers [19], optical comb generation, optical phase arrays [127], and integrated circuits for low-loss optical transceivers [128]. Another promising application is the 3D co-integration of III-V membrane-based optical transceivers onto CMOS or InP-based high-speed electronics. This approach can enable parasitic-free interconnects between photonics and electronic circuits, using lithography-enabled precision and density, at wafer scale [129], [130]. Most importantly, for all of these integration approaches, a key part of the process is the bonding of devices fabricated on two or more different platforms together. This can be achieved by direct bonding [131] or adhesive bonding [132]. Adhesive bonding has advantages for heterogeneous integration as it offers high flexibility in the choice of the bonding layer thickness (10s of nm – 10s of μm), high tolerance to wafer topology, and easy wafer-scale processing [133].

The introduction of the bonding process in the fabrication of heterogeneously integrated devices has opened new possibilities for integration but has also introduced new challenges. One such challenge is the precise alignment of bonded substrates for overlay lithography [134], [135], [136]. While alignment algorithms have advanced in sophistication, the precision of alignment is now confronted by physical mechanisms inherent to the fabrication process, such as wafer warping [137], complex surface topology, or layer dislocations resulting from bonding [138]. These phenomena might be caused by several factors, including non-uniformity of temperature distribution during layer formation, non-uniformity of bonding layer thickness, or mismatched CTEs between different materials [139], [140]. This last factor affects adhesive bonding using BCB, since to cure the BCB, both wafers have to be heated to high temperatures (above 200 °C). For direct bonding using plasma-activated oxides, the situation (*i.e.*, bond temperature) is very similar.

Apart from resulting in mechanical damage to devices when the amount of stress is too high, these distortions also manifest as shifts in the positions of markers during overlay lithography (run-out of overlay error, ROE), e.g., in a DUV scanner lithography tool or mask aligner tool. The distortions that cause ROE contain both linear and non-linear components, as well as residual components that do not fall into the aforementioned categories [141]. While most wafer-scale alignment algorithms can mitigate the linear and non-linear distortions if these are accurately assessed, the residual distortion part remains, leading to poor alignment and subsequently compromised device performance or even wafer rejection by a particular lithography system [142]. In particular, it becomes a challenge to perform the global alignment for overlay lithography before and after bonding due to these membrane distortions [50], [143]. Hence, it is important to investigate the source of these distortions and quantify them to successfully select the right overlay strategies and guarantee high overlay accuracy when needed.

This chapter aims to provide a quantitative analysis of distortions in InP membranes bonded with BCB under different conditions. We define distortion as a physical shift of a point on the membrane surface relative to its position prior to some processing

operation, such as before and after bonding, in a predefined frame of reference. The distortion in a particular wafer region is quantified as a vector value. To fully evaluate these distortions, we used a least-square estimation method to decouple the linear components of distortion in the form of stretching and non-orthogonality from residual distortions which we plot as vector maps across the 3-inch wafer area. Non-linear distortions are not examined as distortions from bonding are dominated by linear distortions. Experimentally, EBL tool is used for marker fabrication and metrology, the displacement of markers after bonding is extracted from the EBL log files, and fitted using a 6-parameter model where both linear and residual components are extracted [143], [144].

The chapter has the following structure. Section 1.1 describes the fitting model that is used to quantify the linear distortions and extract residual distortion maps from the raw data. In section 4.3, we give an overview of the EBL metrology method. The rest of the sections before concluding are dedicated to providing a detailed analysis of data obtained from several experiments. In our first set of experiments, we used Si, InP, 3C-SiC, and glass as carrier substrates to bond with the InP membrane. This allowed us to explore how the membrane distortions are affected by a wide range of CTE mismatch between InP and these carriers, as the bonding is carried out at temperatures above 200°C. The same experiment was carried out to compare different BCB thicknesses in a wide range of 1-12 μm for the case of bonding InP to Si substrate. We also bond an InP wafer with pre-bonding defects and analyze how the presence of those affects both linear and residual distortions. In addition, we demonstrate the presence of residual stress in the membrane, which is the stress that remains after high-temperature processing is finished and one of the substrates is removed. This is realized by etching trenches that separate the 3-inch membrane into smaller areas, and then analyzing the membrane distortions introduced after the etching step. Finally, we propose an alignment strategy that can handle these distortions to achieve high overlay accuracy.

4.2 Description of the fitting model

Overlay lithography distortion patterns represent the displacement of markers from their anticipated positions. These patterns contain both linear and non-linear distortions, as well as residual distortions. In short, linear and non-linear components describe this displacement with linear and non-linear parameters, respectively, while the errors that remain after removing these components from the original distortion pattern are referred to as residual distortions [141]. Hence, it is important to decouple these components and study the main underlying physics that affect them. The goal is to understand the magnitude of these distortions for better overlay compensation on one hand and to improve the fabrication process to limit them on the other. We note that we do not study non-linear distortions in this chapter. We will show throughout the chapter that linear distortions are dominant while residual maps might contain non-linearities that are not significant. Hence, the accurate fitting of the linear distortion parameters and assessment of residual distortion maps is sufficient to encompass membrane distortion and link it to the bonding process.

To decouple wafer-scale linear distortions and extract the residual distortions of the studied samples in this chapter, we used a six-parameter least-square estimation method to fit our data according to the following equations [141]:

$$x_{opt} = x.cos(P_1) - y.sin(P_1) + P_2 + x.(1 + P_4) + y.tan\,(P_6) \qquad (3)$$

$$y_{opt} = x.sin(P_1) + y.cos(P_1) + P_3 + y.(1 + P_5) + x.tan\,(P_6) \qquad (4)$$

Here, P_1 is the rotation in radian. P_2 and P_3 are the shifts (translation) in x- and y-directions in µm, respectively. P_4 and P_5 are the scaling factors in parts-per-million (ppm) in x- and y-directions, respectively. Negative values of P_4 and P_5 point to membrane compression, while positive values point to expansion. P_6 is the non-orthogonality factor in radian. Here, the input marker coordinates (x,y) are fitted to design coordinates (x_0,y_0) and the result of the fitting is the marker coordinates (x_{opt},y_{opt}) that contain all the linear components of the overall distortion. Markers displacement represented by distortion patterns that result from several linear components are shown in Figure 4.1. It should be noted that distortion patterns are typically in the order of a few micrometers/nanometers compared to the 3-inch wafer scale, which necessitates expanding them by orders of magnitude to make them visible. Their magnitude can be assessed by comparison with the scale arrows.

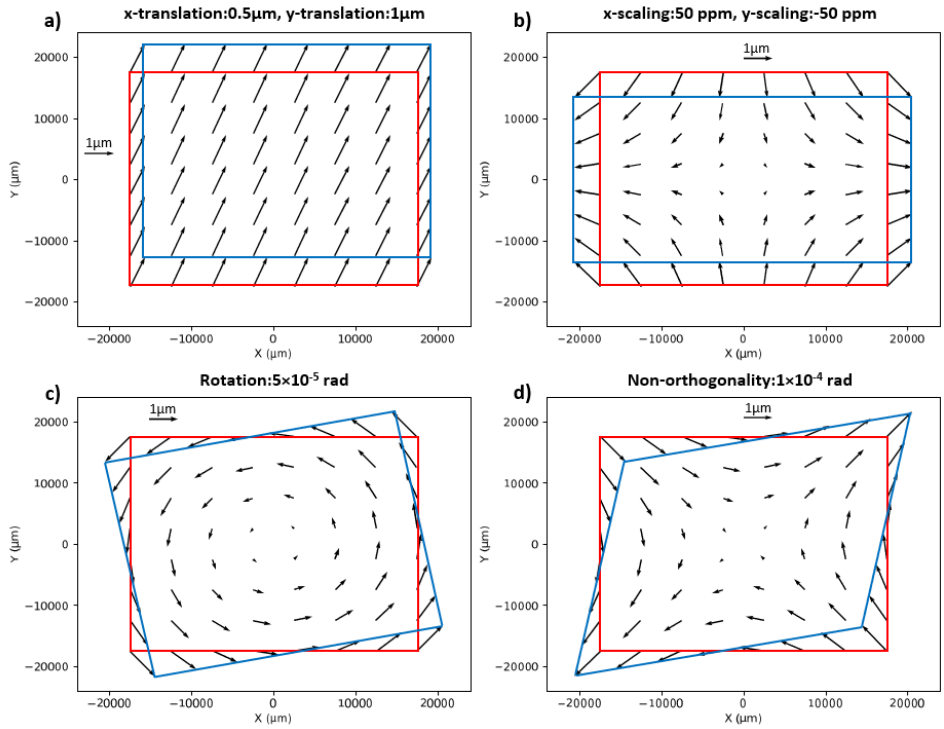

Figure 4.1 Effect of decomposed linear distortions on the displacement of markers

Next, by subtracting the fitted output coordinates (x_{opt},y_{opt}) from the original input coordinates (x,y), the residual distortion pattern is extracted. Throughout this study, we use the standard deviation (STDev) in nm of errors arising from residual components to assess the quality of the fitting, since we fit linear components while the residual components remain as a source of error. Thus, minimization of the STDev is necessary to ensure that the linear and residual distortion components are fully

decoupled. To achieve the best fitting results, several minimization algorithms were tested. We found that the lowest errors can be reached with two algorithms that are suitable for multi-parameter fitting. These are the quasi-Newton method of Broyden, Fletcher, Goldfarb, and Shanno (BFGS) [145] and the trust-region method [145], [146]. Despite that these methods are based on a different rationale for optimization, the obtained values for P_1- P_5 are all similar and within 5% deviation, while the values of P_6 are close to 0. However, we continue with BGFS in this study as it is faster. Moreover, given that overlay systems working on the wafer scale can only compensate for the fitted distortions, the STDev values from residual distortions are representative of the achievable minimum overlay error if all linear distortions are eliminated [141].

Among the linear components P_1-P_6, if the center coordinate of the distortion pattern is not determined precisely, the translation weakly interacts with scaling and the rotation weakly interacts with non-orthogonality. This signifies that careful optimization of the fitting is required to ensure accurate extraction of P_1-P_6 values [141]. In practice, to achieve optimal fitting results of P_1-P_6, we first use a null initial guess for all parameters, and the parameters optimization is bounded with a range that is two orders of magnitude larger than what is physically possible. Next, we feed the model with the optimal translation and rotation values within a lower range to exactly pinpoint the center coordinate and ensure that P_1-P_6 are fully decoupled. After registering the fitted optimal values of P_1-P_6 and the STDev of residual errors in nm, the residual distortions are extracted by subtracting the fitted output coordinates from the original input coordinates. To simplify our terminology, the resulting maps are referred to in this chapter as *distortion maps*, which represent the distortion part that cannot be fitted. Throughout this chapter, only residual distortion maps are shown since the full understanding of linear distortions is captured with the optimal values of P_1-P_6. Moreover, since the parameters (P_1- P_3), *i.e.*, x- and y-translation and substrate rotation, depend on the initial positioning of the substrate relative to the stage [143], these do not contribute to the physical distortion of the membrane and their results are omitted from this chapter. However, we note that their fitted values are very close to the values registered in EBL metrology logs. Accounting for the EBL errors presented in Annex A, the error range of P_4-P_5 is 2ppm and 6ppm and the range for P_6 is 4×10^{-6}rad and 1×10^{-5}rad for results obtained from dedicated fabrication runs and photonic device fabrication runs, respectively. The reason for the higher metrology errors from the latter is the lower frequency of EBL recalibration, which slightly increases the effect of drift. Finally, we note that as long as marker fabrication and reading are possible, this method is applicable to study processing-induced distortions of other membrane materials and systems, and other substrate sizes/dies as well.

4.3 E-beam metrology method

Here we discuss the process flow for our e-beam metrology on adhesively bonded membranes. This study encompasses fabrication runs made specifically for this study employing a standard epi-stack and process flow, which are labeled as *dedicated* runs. We also used results from functional photonic device fabrication runs, within which the bonding is a small part of the entire process flow required to fabricate functional devices. So the main goal of using the other runs is to assess the fitting model on complex fabrication schemes, and to verify that the bonding parameters that affect membrane distortion also extend to photonic device fabrication schemes. To simplify

the fabrication flow, we only detail the common steps between dedicated and functional photonics runs while other steps are described in general. A simplified process flow is shown in Figure 4.2. For dedicated runs the standard epi-stack consists of 300 nm InP and 300 nm InGaAs etch-stop layer, yielding a membrane thickness of 300 nm after bonding and subsequent removal of InP substrate and InGaAs etch-stop. For functional photonics fabrication runs, the stack thickness can vary between 300 to 1500 nm of III-V semiconductor multi-layers depending on their functionality. Their final fab-out membrane thickness is usually close to these thicknesses since most of the semiconductor materials remain after fabrication. We note that the markers used in both dedicated and functional photonics runs are *negative* markers since they yield lower beam intensity than their surroundings during e-beam reading. However, we also describe the flow for fabricating *positive* Au markers, which are used in one experiment to study the relationship between InP membrane stress and distortion. For the carrier substrates' choice, we required a sufficiently wide range of CTE mismatch between the InP membrane and carrier substrate. Hence, the chosen substrates are: InP with identical CTE to the InP membrane of 4.75×10^{-6}/°C [147], Si and 3C-SiC with CTEs of 2.55×10^{-6}/°C [148] and 2.77×10^{-6}/°C [149], respectively, and finally glass substrate with a low CTE of 4.8×10^{-7}/°C [150].

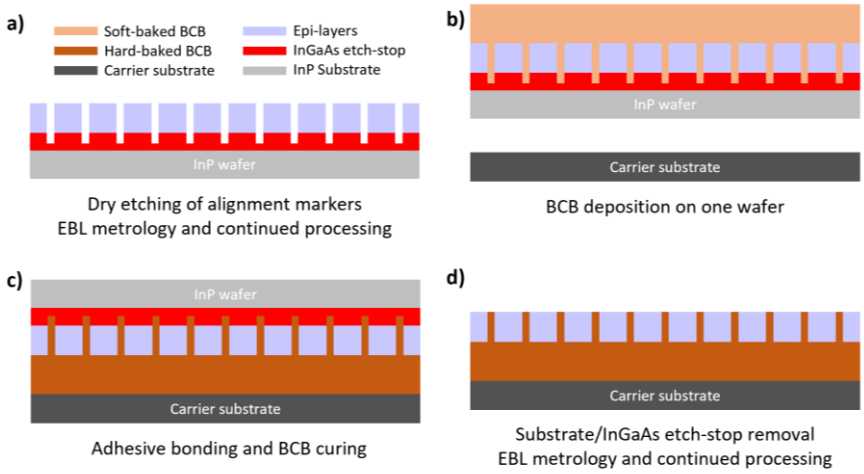

Figure 4.2 Simplified process flow steps relevant to this study, a): marker fabrication, b) substrates preparation for bonding, c): Adhesive bonding, d): InP substrate and etch-stop layer removal

The fabrication starts with creating markers where we deposit 50 nm of PECVD SiN as hard mask for dry etching. The mask is coated with ZEP520A resist and patterned with EBL. The nitride is then dry etched in pure CHF_3 RIE plasma. Next, we deeply etch into the epi-layers using CH_4/H_2 ICP RIE plasma until the InGaAs etch-stop is shallowly etched to guarantee visible markers after bonding. Similarly, the experiment with positive markers only differs in the marker fabrication stage where we use a lift-off process of 50/100/50 nm Ti/Au/Ti stack. Ti is used for optimal adhesion to the BCB and the substrate. Next, we read these markers in EBL to obtain the pre-bond analysis data (Figure 4.2.a). For functional photonics wafer runs, other pre-bonding device

fabrication processes follow at this stage, which include metal deposition and rapid thermal annealing, semiconductor dry and wet etching, and permanent oxide deposition. These processes mainly affect the topography and residual stress of the InP wafer to be bonded, which can yield different results compared to the dedicated runs. Next, we prepare for bonding by depositing PECVD SiO_2 on both the InP wafer and the carrier substrate and follow it by spin-coating AP3000 and baking it at 135°C to promote adhesion. We subsequently spin-coat BCB on the InP wafer and soft-bake it at 100°C, which achieves a flat top surface (Figure 4.2.b). The latter can require BCB thicknesses up to a few tens of μm if the initial device topography is high [151]. Therefore, the investigated thicknesses are 1μm, 2μm, and 12μm. The corresponding BCB to these thicknesses are Cyclotene 3022–35, −46, and −63, respectively. We note that unless otherwise specified the default thickness is 2μm since it is the most often used for functional photonics membranes, and in other platforms as well [50].

Next, we align the wafers by their major flats in a commercial EVG620 aligner and lock them into a cassette holder, which is transferred to EVG520 bonding tool. For bonding, we use a force of 700N under vacuum and a low ramp rate of 5°C/min until 280°C is reached and stabilized for 1hr to fully cross-link the BCB material (Figure 4.2.c). During bonding, the temperature uniformity is high since the top and bottom parts of the bonder are controlled separately within 0.1°C difference. After bonding, the InP substrate and InGaAs etch-stop layer are wet etched in $HCl:H_2O$ and $H_2SO_4:H_3PO_4:H_2O$, respectively (Figure 4.2.d). For InP carrier substrates, we use protective multi-layer coatings to preserve the carrier substrate during wet etching and then remove these coatings afterward [130]. The precise coordinates of the markers are then read out using EBL to assess the effect of bonding on membrane distortion. Moreover, although the thickness non-uniformity of BCB before bonding is below 5%, the latter can increase drastically after bonding because BCB becomes liquid and can reflow during bonding [135]. Hence, reflectometry was used to extract the post-bonding BCB thickness non-uniformity maps for further analysis.

The EBL we used is Raith EBPG5150. Before lithography or metrology, the sample is placed onto a 3" holder that secures it against three pins from the top surface by clamping it from the backside with a spring mechanism. The locations of the 3 pins are shown in Annex A. This EBL fixing mechanism differs from other lithography tools that secure the sample to the holder with vacuum and fully flatten it. After loading the holder into the loadlock and reaching $\sim 10^{-7}$ mbar of vacuum, the holder is transferred to the EBL chamber where lithography (marker fabrication) or metrology (marker reading) is carried out. The system is configured to recognize square 20×20 μm^2 markers. The markers are distributed across the full 3" wafer area in all experiments. To investigate the influence of mapping resolution on the accuracy of analysis, the dedicated runs contain maps of markers with three uniform pitch selections in the (x,y) directions. Note that the x- and y-directions are perpendicular and parallel to the major wafer flat, respectively. The pitches in (x,y) coordinates are 5mm by 5mm labeled as *coarse* maps that contain ~100 markers, 2.5mm by 2.5mm labeled as *fine* maps containing ~600 markers, and 1.25mm by 1.25mm labeled as *ultra-fine* maps containing ~1800 markers. Wafers from photonic device runs use a pitch of ~6×8mm^2 with a similar resolution to the coarse maps.

To choose optimal beam parameters for our study, we investigated the influence of those on the markers reading/writing accuracy and repeatability using a bare 3" wafer. The goal is to measure systematic errors to ensure the accuracy of results in the

following sections. The main EBL systematic errors arise from beam drift and current used during marker lithography/metrology [152]. Therefore, we investigated beam currents in a large range of 5-190 nA. Evaluation of the EBL metrology accuracy shows that using smaller beams (low beam current) and averaging the data from several readings of the same marker slightly increases the accuracy of results. More details can be found in Annex A. Based on this, we chose the optimal beam currents of 100 nA for lithography and 5nA for metrology for dedicated runs, while functional photonics runs use similar currents. For metrology, after an EBL job is carried out, we use its log to extract the found marker positions and all relevant details that are used for analysis, the data is then fitted to extract linear and residual components of the distortion as described earlier. We note that distortions induced by the pins are spotted close to pin locations in all of our maps, even rotating the wafer 90° with respect to the holder resulted in the same distortions, and an example of these patterns is shown in Annex A. Most importantly, these are minimal compared to the linear and residual distortions after bonding, and hence their influence is minimal on the derived values. These distortions might result from wafer bow variations between processes, since the latter is not fully neutralized on the wafer scale by the pins.

4.4 Benchmark analysis of membrane distortions after bonding

To better explain the different distortions, we first present a baseline experiment where a 300nm-thick InP membrane is bonded to Si using 12µm BCB. The reason for choosing 12µm BCB as baseline is that it is suitable for the co-integration of electronics with photonics. The bonding temperature is 280 °C for 1h. Figure 4.3.a shows the pre-bond residual distortion map. The found values of the x- and y-scaling are 2.7±1ppm and 0.9±1ppm, respectively. The non-orthogonality is found to be 3.4×10^{-6} rad, while STDev of residual errors is 22.1 nm. This indicates that the found marker positions are slightly distorted in the order of a few tens of nm from the design map. The map in Figure 4.3.a shows that the displacement of markers in the edge contributes more to the residual distortions. The reason might be the presence of non-uniform residual stress during lithography, which is released after SiN removal and e-beam metrology, for instance, because of the 2-dimensional bow profile. Further details and explanations on this can be found in (Annex A). The inset in Figure 4.3.a shows bell plots representing the distribution of found marker positions relative to the design coordinates for the pre-bond and post-bond maps. STDev increases significantly after bonding in comparison to the pre-bond case, so residual distortions are more present in the post-bond case. For the post-bond experiment, fitting with methods BFGS and trust-construct yield x-scaling values of 323.461±1ppm and 323.462±1ppm, y-scaling value of 322.910±1ppm and 323.075±1ppm, non-orthogonality value of $1.14\pm2\times10^{-6}$rad and $1.13\pm2\times10^{-6}$rad, and STDev values of 104.26 nm and 104.28 nm, respectively. This is consistent with other wafers studied in this chapter, and similar scaling values were reported as well [50]. The residuals map (vectors) aligned to the BCB thickness uniformity map (colored map) is shown in Figure 4.3.b. It can be seen that the length of the vectors increases by a factor of three and the position of the longest vectors is present in the center as well as in the edge compared to the pre-bond map, suggesting that these residual distortions are linked to the bonding process.

We note that expansion values above 500 ppm can start to interfere with the light emission properties of III-V-based semiconductors [153]. Despite that the presented values are below this threshold, they might still need to be taken into account when designing devices where small values of strain play an important role in the device performance. For instance, for a polarization-insensitive semiconductor optical amplifiers working in the O-band, a value of 300 ppm in strain represents a 15% increase from the desired strain for optimal polarization insensitivity [81].

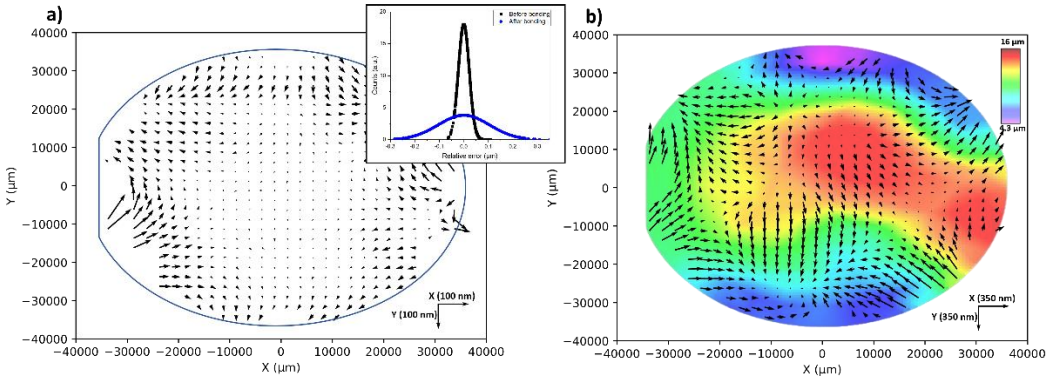

Figure 4.3 a): Pre-bond distortion map of the InP wafer, inset: bell plots of residual errors before and after bonding, b): post-bond distortion map of the InP membrane overlapped with the thickness variation map from reflectometry

4.5 Effect of BCB thickness and thickness non-uniformities on distortions

Figure 4.4 shows results obtained on membrane scaling in both directions and non-orthogonality for InP membranes bonded on Si with different BCB thicknesses. Each point in the x-scaling, y-scaling, and non-orthogonality represents one bonding experiment with negative markers. The values enclosed by a black circle are extracted from dedicated runs while the rest are from functional photonics runs. The values of x-scaling are within 316-322ppm for BCB thicknesses of 1 and 2 µm and slightly increase up to 323 ppm for 12 µm BCB. Similarly, the values for y-scaling increase from the range of 303-307 ppm for 1 µm BCB to 306-310 ppm for 2 µm BCB, and up to ~322 ppm for BCB thickness of 12 µm. Across all of our measurements, the x-scaling is higher than the y-scaling. This difference is below 1ppm for bonding with 12µm BCB and amounts to values up to 15ppm for experiments with BCB thickness below 2 µm. The mechanism behind this anisotropic expansion is unclear. It might be the result of an anisotropic distribution of forces during the bonding or the presence of an anisotropic behavior in the CTE or the mechanical properties of the substrate carriers. In either case, higher BCB thicknesses help in the reflow of BCB during bonding to better accommodate for these residual stresses, which might be the reason why this anisotropy is lower in the experiment with 12 µm BCB compared to lower thicknesses [110]. As for non-orthogonality, we found no correlation between its variation *vs* BCB thickness based on the results presented in Figure 4.4.b, especially given the high variation of non-orthogonality from sample to sample for BCB thickness below 2 µm. This variation and the variation of x- and y-scaling factors across samples might be linked to the different

pre-bonding and post-bonding processing steps that the samples went through and/or the thickness variations of the membrane.

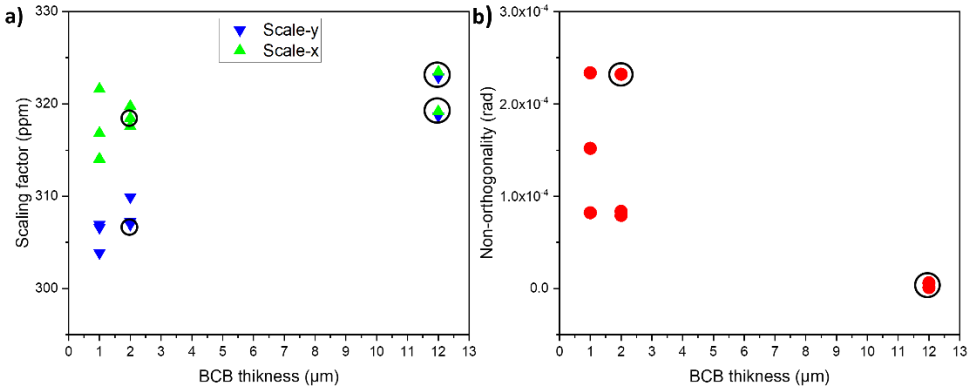

Figure 4.4 Linear distortions of the InP membrane *vs* BCB thickness, a): x- and y-scaling factors, b): non-orthogonality. Circled data points represent dedicated wafer runs, while the rest are from other functional photonics runs

We also bonded InP with 90° angle mismatch between the membrane and the Si wafer to see its effects on the values presented earlier. The BCB thickness is 2µm and the wafer was read with the Si flat facing the direction used in all other experiments. A post-bond picture and distortion map of the wafer are shown in (Annex A). Results of the fitting are 325.112±1 ppm, 317.741±1 ppm, and $1.659±2\times10^{-6}$ rad for x-scaling, y-scaling, and non-orthogonality, respectively. The x and y directions are defined with respect to the carrier Si substrate for direct comparison with earlier experiments. Here, x-scaling remains higher than y-scaling similar to earlier experiments but with a slightly lower value difference of 7-8 ppm compared to earlier values in the range of 10-15 ppm for the same BCB thickness. This suggests that the distortion is not dependent on the relative orientations between the two wafers. The slight difference is linked more to an anisotropic behavior in the bonding forces or the Si carrier relative to the InP membrane. The latter might be the reason why this difference in the 12 µm BCB sample is low since the separation between the membrane and Si is higher. To further study this, we analyzed the thickness non-uniformity results from the dedicated 12 µm BCB wafer (Figure 4.3.b). Here, the vector direction and length slightly correspond to the direction where the BCB thickness changes more abruptly in the thickness map. However, the full distortion map and thickness variation map do not entirely overlap, hinting that other effects also take place. This might be related to the inherent residual stress present in all measurements, or more likely the presence of residual stresses during/after bonding. However, these effects do not induce significant distortions as compared to the linear scaling factors that we found in our experiments.

4.6 Effect of substrate materials

Carrier substrates for membrane photonics are usually chosen for their functionality. However, the substrate choice is crucial for the success of integration with adhesive bonding [110]. This is because the substrates and the membrane are bonded at temperatures above 200 °C. Thus, their CTE mismatch results in residual stresses and

membrane distortion after bonding when the temperature falls back to room temperature. An equation to describe membrane scaling *vs* CTE is given as follows:

$$P = \Delta T . \Delta \alpha \quad (5)$$

Here, P can be the average of P_4 and P_5, ΔT is the bonding temperature minus room temperature, and Δα is the CTE mismatch. To investigate the effect of substrate choice on the scaling in x- and y- directions, we first calculated the theoretical values of scaling for InP membrane for different carrier substrates and for bonding temperatures of 250°C and 280°C, which are most often used in literature [110]. We also plotted the average of P_4 and P_5 from our experiments where the BCB thickness is 2 µm and the bonding temperature is 280 °C. Results are shown in Figure 4.5.a. The thermal expansion of InP is higher than all other substrates used in this study, which is why the membrane scaling here is limited to expansion (positive values of P_4 and P_5). In the case of bonding InP to InP carrier, a CTE mismatch of 0 is calculated from theory. However, our experimental findings reveal an average scaling factor of 4.53±1 ppm. This points to the presence of expansion within the InP membrane, even for InP to InP bonding. This expansion is likely attributed to the partial relaxation of residual stresses that may exist in the BCB layer, which are around 40 MPa, as discussed in Chapter 3. This situation likely arises due to the significantly higher thermal expansion of BCB as a polymer compared to InP and other semiconductors. Consequently, the residual stresses that accumulate within the BCB layer could potentially impact the InP membrane more significantly than the underlying InP substrate. The latter is due to the substantial difference in thickness between the substrate and the membrane, with the substrate being three orders of magnitude thicker.

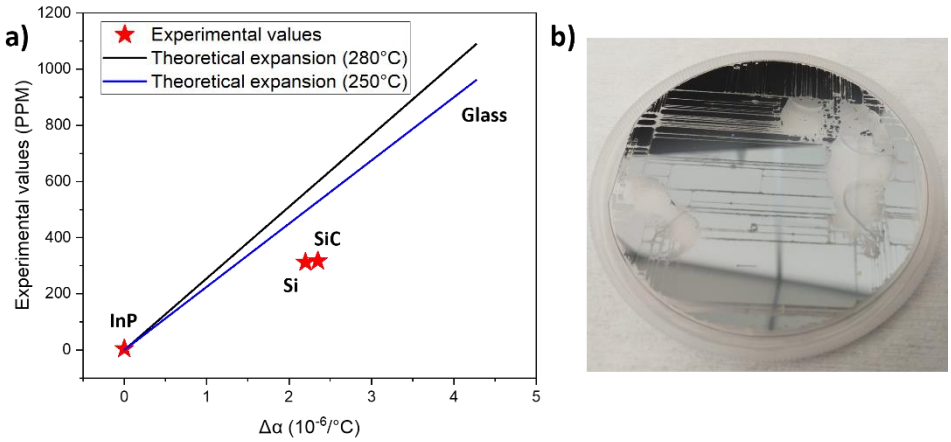

Figure 4.5 Calculated and experimental values of the InP membrane expansion *vs* CTE mismatch, b) image of the bonded membrane-on-glass before removal of the InGaAs etch stop

The average scaling factors measured on Si and SiC wafers are 312.4±1 and 317±1 ppm, respectively. These values are consistent with a multitude of photonic device runs on Si that are not presented [21], [105], and also InP electronics on Si [50]. These values deviate by 248.6±1 and 282.2±1 ppm from the anticipated theoretical expansion values. Therefore, it is reasonable to suspect that this difference in the expansion was liberated

after bonding as residual stress. To better explain this, we deconstruct the expansion of the membrane into two distinct segments. The values acquired through experimentation, denoted as P_4 and P_5, are designated as *residual expansion*, while the variance between the experimental and theoretical values is termed *released expansion*.

It is possible that the released expansion results from the relatively higher elastic deformation of BCB in comparison to the InP semiconductor membrane on top [110]. Another explanation for the significant difference between experimental and theoretical values could be related to the crosslinking of BCB during the temperature ramp-up phase of the bonding. It is plausible that a point of permanent adhesion between the two wafers on the wafer scale occurs before 100% crosslinking in BCB that is achieved at 280 °C. A calculated temperature based on experimental data and matched to our thermal ramp-up yields a value >170 °C for this occurrence, with the degree of crosslinking during the slow ramp-up remaining slightly below 50% [110]. Hence, this could potentially co-exist with the previously mentioned mechanism, and is further supported by experiments in section 4.7. In Figure 4.5.b, an image depicting the bonding outcome to the SiO_2 substrate is presented. Alongside the noticeable locations indicating membrane detachment, there are discernible vertical and horizontal lines. These are only visible after the removal of the InP substrate. Theoretically, the membrane should experience an expansion of 1088.9 ppm due to the substantial CTE mismatch of an order of magnitude between InP and glass. The presence of such lines, where the InP membrane has split, suggests that the extent of released expansion surpasses the values previously observed for Si, which would require plastic deformation of the membrane and therefore formation of these lines. Although extraction of the values of P_4 and P_5 was not possible as a result of the membrane damage, these should be much higher than the largest values of 325±1 ppm recorded in this study to cause the membrane to rupture, which underscores the necessity for a more customized bonding approach for materials with high CTE mismatch. Finally, we note that in these experiments P_4 is also higher than P_5 by 11.22±2 ppm, 7.19±2 ppm, and 5.14±2 ppm for Si, SiC, and InP substrates, respectively. These values seem to increase with the CTE mismatch, which further confirms that it is more related to the bonding or the properties of the carrier substrate.

4.7 Effect of residual stresses

Here, we investigated the presence of residual stresses on the InP membrane to evaluate its effect on distortions and to distinguish it from the effects mentioned in section 4.6. For this, we used the bonded sample with results shown in Figure 4.3 where we further etched the InP membrane into isolated areas of different sizes, as shown in Figure 4.6. The lines are fully etched through the InP membrane, and are 50 μm in width to ensure accommodation of any deformations resulting from stress release. For the layout, the top-right part was left pristine as a full quarter, the top-left quarter of the wafer contains 10×10 mm^2 squares, and the bottom part was etched into 5×5 mm^2 squares. The goal is to investigate the effect of residual stress alone. Here, as the residual stress distributes across the full scale of the membrane, etching smaller isolated areas leads to a redistribution of residual stress across each area. This residual stress redistribution depends on the sizes of the isolated areas as well [154]. Thus, we fitted each part individually where (x_0, y_0) are the post-bond positions before etching (membrane intact) and (x, y) are the post-bond positions after etching, *i.e.*, the

membrane is cut according to the lines. We found that the x-scaling and y-scaling factors of the three regions are all within 2 ppm of the original map positions before cutting, and their non-orthogonality is below 5×10^{-6} rad from the original map positions. This signifies that the residual stress from the InP membrane has a low impact on the linear distortions, which is in the order of a few micrometers. However, the residual distortion shows a completely different behavior. Figure 4.6.a represents the distortion map for the different regions. The arrows representing distortions lying in 5×5 mm^2 and 10×10 mm^2 cut areas have a higher magnitude compared to the top-right quarter where the membrane is left intact. This suggests that a part of the residual stress in these regions is released as strain, leading to a displacement of the separated small square membranes individually. This is also reflected on the STDev values of errors, which are 43.7 nm, 40.8 nm, and 16.2 nm, for regions with 5×5 mm^2 square separations, 10×10 mm^2 square separations, and no square separation, respectively.

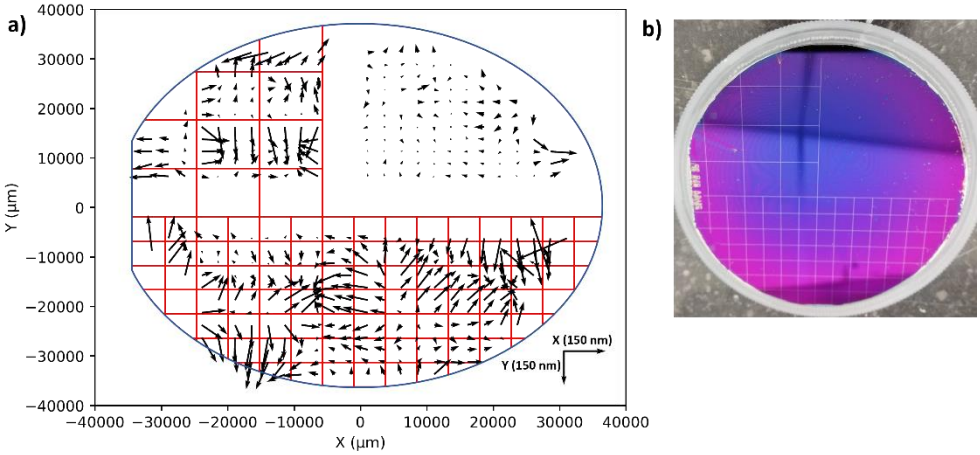

Figure 4.6 Post-etch distortion map of the InP membrane-on-Si, b) image of the InP cutting pattern on ZEP520A resist before etching

As mentioned in section 4.6, the measured distortion scaling factors of InP-on-Si and InP-on-SiC are noticeably below what is expected from theoretical calculations. This was linked to two possible coexisting mechanisms with residual stress from the membrane being one of those. Thus, releasing the residual stress induced by the InP membrane can reveal its contribution to both linear and residual distortions. To further investigate this, we performed a bonding experiment of an InP membrane with Au markers (*i.e.*, positive markers) on top of Si, so that the InP membrane can be totally removed and only the BCB layer with Au markers remains. The bonding parameters remain the same compared to the experiment shown in section 4.4, *i.e.*, we bond with 12 µm BCB on a Si substrate and at 280 °C. After bonding, substrate removal, and the complete removal of the InP membrane with wet etching, metrology is carried out and marker locations are extracted and fitted with the model. For linear distortions, we found values of 326.63±1 ppm for x-scaling, 315.93±1 ppm for y-scaling, and $3.1\pm3\times10^{-6}$ for non-orthogonality, which are comparable to the values obtained with negative markers in section 4.4. This signifies that the contribution of residual stress from the InP membrane to the difference between theoretical and expected scaling values shown in the previous section is much weaker compared to the other mechanism. Thus, the

deviation of values from theory seen in section 4.6 of >240 ppm is likely linked to the permanent adhesion of the two substrates at a lower crosslinking percentage of BCB than the expected value of 100% crosslinking. We also note that the difference between x-scaling and y-scaling is ~10.7±2 ppm here, which is significantly higher than the value <1ppm from the previous experiment, suggesting that the anisotropic behavior that is witnessed in these samples mainly arises from the substrate carrier. We also note that the STDev here is ~30% higher than in previous the experiment, suggesting that more residual errors arise after the removal of the membrane. However, this might be related to the difference in BCB non-uniformity values in the two experiments as seen in the BCB thickness non-uniformity maps (Figure 4.7 *vs* Figure 4.3.b). In Figure 4.7, saddle points visible in the distortion map correlate with small gradients in the BCB thickness while higher distortions correlate with strong gradients in BCB thickness. These gradients arise during the BCB reflow between two plain wafers under pressure, and are caused by non-uniformity of the bonding forces, such as non-planarity of the bonding glass and unequal forces applied from two pins on each side of the bonding cassette.

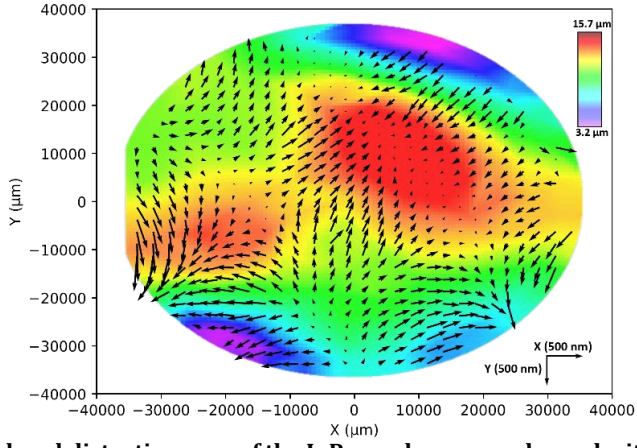

Figure 4.7 Post-bond distortion map of the InP membrane overlapped with BCB thickness variation map for the wafer with 12µm BCB thickness and Au markers (the InP membrane is completely removed)

Finally, we note that the dominant distortion in this study is the scaling, with values consistently found in the 300-330ppm range throughout all of the differently processed wafers, except for bonding on InP substrate revealing almost no scaling. For device fabrication on InP membranes containing distortions, the large parts of linear distortions can be corrected in the design phase to lower the overall distortions from a few micrometers to the sub-micrometer level, while the non-linear residual distortions can be corrected by the alignment schemes of the advanced optical lithography tools, such as the Argon Fluoride (ArF) scanner. The latter uses a similar mechanism to EBL where local distortions are compensated for in local cell exposures. Functional InP membrane photonics on Si substrate fabricated with EBL were consistently demonstrated [68]. Their fabrication involves double-side processing before and after bonding where EBL corrects for the local distortions before exposing the cell, hence achieving overlay accuracy below 20 nm. For the vertical integration of membrane

photonics on top of electronics substrates, we note that the post-bond alignment, *i.e.*, translation and rotation between the two substrates, can be preserved without influencing the bonding parameters by introducing hard pillars from the photonics side to avoid slippage (Chapter 3). Moreover, distortion of the electronics substrate is negligible compared to the membrane photonics by view of its three orders of magnitude larger thickness. Thus, taking all of these points into consideration could enable the intended application of photonics and electronics co-integration.

This overlay strategy has also been reported in the fabrication process of InP electronics on Si electronics, where the large part of scaling is corrected by scaling the design, and the distortions that are left are corrected by the lithography tool [50]. Moreover, we recently fabricated photonics where an optical lithography tool was required for a post-bond lithography. The optical mask used must be pre-compensated with anticipated expansion. To generate the mask, we read and fitted our post-bond distortion data, and corrected for the linear part. The overlay pattern across different positions from the wafer is shown in Figure 4.8. These indicate that the large part of distortions, which is in the order of 10µm for edge markers, is corrected to lesser than 1µm.

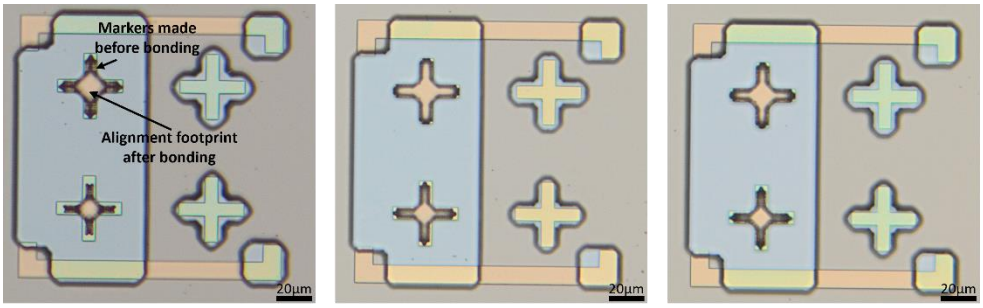

Figure 4.8 Overlay alignment patterns from three different locations in the fabricated wafer, with the designs compensated for the scaling.

4.8 Effect of defects

The presence of defects, such as large hard inorganic particles and epitaxial defects, have been shown to affect post-bonding distortions on the scale of the full intact membrane area for direct bonding techniques [143]. Bonding with BCB is usually more tolerant to these defects. This is why it is important to assess the effect of the local presence of defects on the linear and residual components of distortion in this study. Knowledge of the extent of this distortion is crucial to deciding on post-bonding lithography strategies that can account for these errors. To test this, we used a wafer with an epitaxial defect located in the center of the wafer with topography above 2 µm, and the wafer was bonded to Si with 2 µm BCB. After bonding and substrate removal, the membrane was found to be cracked in the center along the y-direction (Figure 4.9.a). The crack originated from the defect. Its vertical propagation is highly likely due to the stress from pins used to hold the bonding stack inside the bonding cassette, which are located on the top and bottom sides of the wafer. We first fitted the full map to assess the distortion. Figure 4.9.a shows the post-bonding distortion map where all markers

were fitted at the same time. The line where the membrane broke is visible both in the microscope and in the map and the extra separation between markers at the two sides of the line is around 10 µm. This high separation is most likely linked to the formation of a crack during the bonding phase. We also fitted the right and left sides of the maps separately to extract the residual distortion maps, results are shown in Figure 4.9.b. The STDev of errors in nm for both maps are similar to results obtained in section 4.6. The x- and y-scaling factors are found to be 312.9±1, 318.5±1 ppm for the right map, and 313.8±1,329.7±1 ppm for the left map, respectively. Values of x-scaling are slightly smaller than previous values of similar experiments by 5±2 ppm. Moreover, the map in Figure 4.9.b shows that the vectors near the cleaved line and particularly near the defect are larger than in the center of the two separate membranes. These observations point to a redistribution of the membrane residual stress on the wafer level. Hence, the presence of such defects can be detrimental to overlay lithography both when compensating for linear distortions alone and afterward when dealing with residual distortions that increase the minimum achievable overlay error.

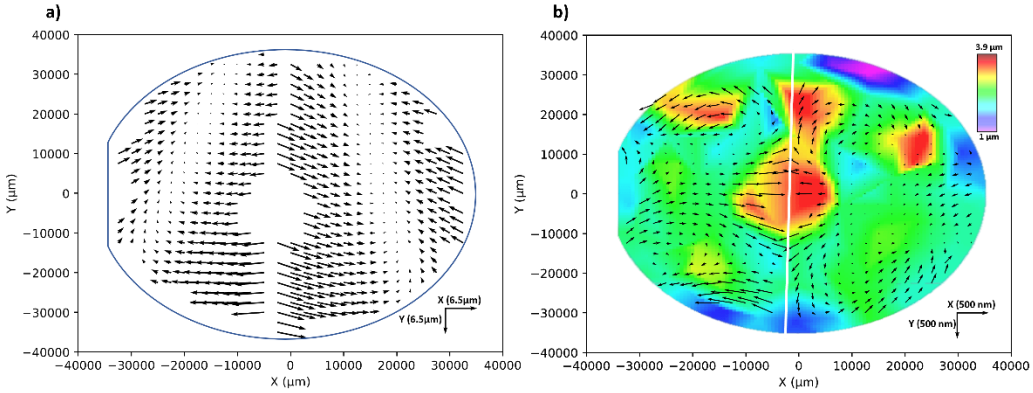

Figure 4.9 Post-bond distortion map of the defective InP membrane: a): with full wafer fitting, b): overlapped with BCB thickness variation with fitting left and right membranes separately

4.9 Conclusion

In this study, we developed a general method with high accuracy to analyze linear and residual distortions in membrane layers for 3D integration. We used the method to investigate the deformation of InP membranes resulting from wafer-scale bonding with BCB. Various angles of the bonding process have been investigated, revealing key factors affecting membrane distortion. We found that linear distortions are mostly affected by the CTE mismatch of bonding substrates (such as Si, InP, SiC, and glass), in a large expansion range of 0-325 ppm, while residual distortions depend on a multiplicity of factors. These are found to correlate with the post-bond BCB thickness non-uniformity and InP membrane residual stress. We also observed that the presence of defects influences all distortions on the wafer scale, which can be detrimental to overlay lithography for membrane devices. By accurately quantifying these distortions, high throughput fabrication of heterogeneous InP devices can be enabled.

5

Chapter 5
Technology development

3D integration of nanophotonic devices onto EICs presents a promising pathway for advancing compact and scalable SoCs. However, the viability of this method depends on preserving the energy efficiency and functionality of photonic devices on top of the membrane. The high BCB thickness required for void-free bonding isolates active photonic devices from the heat sink, which localizes their heat to the diode region and affects their energy efficiency. This chapter focuses on technology development required to tackle this challenge by presenting the design and detailed fabrication flow of active devices with improved thermal managements. These devices are SOAs, DFBs, and UTC-PDs that feature a thermal shunt to connect their heating core to the actively cooled substrate.

The chapter is structured as follows. First, we discuss the modifications required in the fabrication flow to incorporate thermal shunt on SOA/DFBs and UTC-PDs. These developments focus on compatibility with the 3D co-integration process outlined in Chapter 2. Next, we address the specific challenges in measuring the energy efficiency of DFB lasers, emphasizing the importance of tailoring the coupling coefficient and accurately calibrating passive optical losses. Finally, we introduce the development of on-membrane resistors, which play a crucial role in the 3D E-PIC receiver SoC discussed in Chapter 8.

5.1 Design and fabrication of thermally shunted SOAs/DFBs on IMOS

5.1.1 Design and fabrication flow

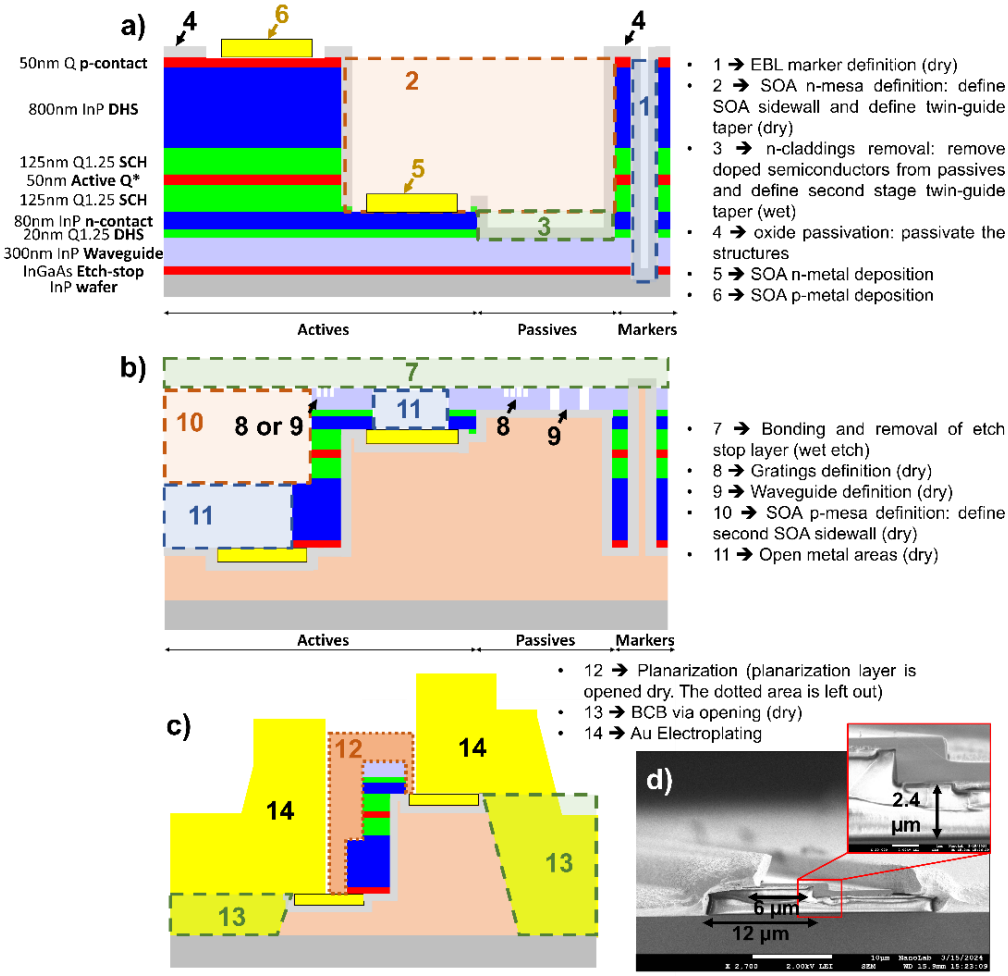

Figure 5.1 Schematics illustrating the key fabrication stages of thermally shunted DFBs (dashed lines represent etched areas). a) right before bonding, b) after bonding and actives/passives definition and metal open. c) after TPV open and plating (final structure). e) cross-sectional SEM image of the DFB with a zoom-in picture of the diode core.

For the study presented in Chapter 6, two types of devices were fabricated in view of thermal management. We refer to heat isolated devices as reference devices, while devices thermally connected to the substrate are referred to as shunted devices. Note that shunted devices have a thermal connection on both the p- and n-side of the diode, as in Figure 5.1.d. Schematics after key DFB/SOA processing steps are shown in Figure 5.1. The epi-stack design is shown in Figure 5.1.a). The functionality of each layer is fully discussed in Chapter 7 to avoid redundancy. The flow consists of a modified flow for the

fabrication of S-shaped twin-guide SOAs described in [78], [155]. Modifications address the necessary tolerances that thermal shunts require, and outcomes from the compatibility study with 3D integration onto electronics described in Chapter 2. Details on modified or new process flow steps are provided next.

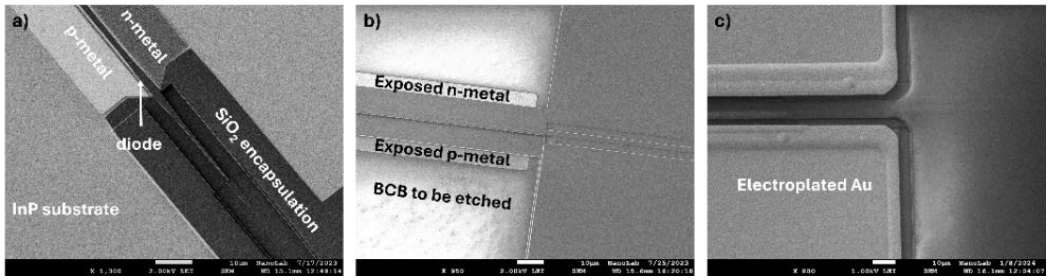

Figure 5.2 SEM images of a shunted DFB: a) just before bonding (step 6), b) after bonding and semiconductors removal for exposing contacts (step 11), c) after BCB etching and Au electroplating

SEM images of after key fabrication steps (step 6,11, and 14 in Figure 5.1) in the fabrication of shunted DFBs are shown in Figure 5.2. Figure 5.2.a) shows the SOA/DFB diode area just before bonding. Here, the diode n-mesa is defined along with twin-guide tapers in step 2, the doped layers are removed from passives in step 3, the SiO_2 passivation layer is deposited in step 4, and n- and p-contacts are deposited in step 5 and 6, respectively. A 12μm width of p- and n-contacts is chosen, and the reason for this is explained next. Figure 5.2.b) shows the structure after exposing the contacts in step 11. Bonding and removal of the etch stop layer is realized in step 7. The used carrier substrate is extremely high resistivity Si (> 20.000 Ω.cm) to avoid creating a short circuit between the two shunts. Next, the waveguide and gratings are dry etched in step 8 and 9, respectively. The second SOA mesa sidewall is etched in step 10, while the semiconductor layers are cleared to expose the metals in step 11. We expose only 6μm of the total metal width for sufficient overlap between these initial contacts and the plated metal deposited later. The rest 6μm of the metal in Figure 5.2.b) is buried under the n- and p- semiconductors. The transfer length is smaller than 6μm, so this metal-semiconductor overlap does not degrade electrical injection into the diode compared to the overlap of 20μm used in reference devices. Additionally, at step 11, the rest of the pad area only has BCB that will be etched to create TPVs. Figure 5.2.c) shows the plated Au connecting the diode to the Si substrate. Here, a BCB planarization layer is deposited and etched in step 12 and the bonding BCB is etched in step 13. Finally, the Au is plated in step 14.

Patterning in steps 12-14 is realized using optical lithography instead of EBL. The choice of 12μm width of initial contacts stems from the fabrication tolerances using optical lithography discussed in Chapter 4. Hence, the final achieved effective thermal distance between the heat-generating core and the Si substrate is the same, while the distance between the shunt wall and the diode core is 6μm (Figure 5.1.e). Both of these values could be significantly reduced by using laser writing or EBL. This can further improve the shunt performance, so these effects are comprehensively analyzed via simulations presented in Annex B. Further fabrication details follow next.

Note that for step 2, O-band SOAs require a taper tip of 100nm instead of 200nm [81]. This is achieved by improving the dose and e-beam exposure settings. Also, separate confinement heterostructure (SCH) layers for the O-band stack use Q1.05 instead of Q1.25 used for C-band. This is problematic for step 3. This step is realized with wet etching using Piranha. However, the etch rate drops from 100nm/min for Q1.25 to below 20nm/min for Q1.05. Consequently, the etch time significantly increases and can affect other structures if not covered properly. Dry etching should be used for this step in future fabrication.

For step 8 and 9, the etch depth is 120 nm for gratings used for I/O GCs, and 300 nm for passive waveguide definition. These steps can also be used to inscribe gratings on top of the SOA top surface to fabricate DFBs. Here, the 120 nm and 300 nm etch depths are used to inscribe shallow and deep gratings, respectively. The characteristics of these gratings are detailed in Section 5.1.2. Also note that for metal opening (step 11), etching is carried out using dry etching instead of wet etching, because the semiconductor openings for shunted DFBs are much closer to the SOA mesa compared to reference DFBs as discussed earlier. Dry etching here provides more process tolerance.

Steps for making shunts are highlighted in Figure 5.1.c) and are further detailed in the following paragraphs. For step 12, the planarization layer provides a degree of freedom where DC and RF transmission lines can be routed between components as well as toward pads near the PIC edges for packaging. For RF signals, the layer provides a separation between RF interconnects and active photonic devices having doped semiconductor layers, hence achieving low RF losses. Note that we chose BCB instead of planarizing with polyimide. This is because BCB is baked at 240-250 °C in comparison with polyimide that needs to be baked at 375°C. This is because processing temperatures below 250 °C are required to preserve EIC devices (Chapter 2). BCB is also ideal for planarizing trenches, and its chemical stability is also better [156]. Thus, the process is tailored to be compatible with EICs. For the deposition, we start with 50 nm of SiO_2 and outgassing at 250°C for 1h, followed by 1µm thick BCB and baking at 250°C for 1h as well. Though, the temperature can be lowered to 240°C for 4h total. Note that the required degree of cure needed for planarization BCB is lower than for bonding BCB. Next, we deposit an adhesion promotor and AZ9260 resist. Optical lithography is then realized followed by etching in CHF_3/O_2 5:1 plasma, with a selectivity between BCB and SiO_2 of 8:1. The resist is then removed in acetone and IPA followed by O_2 plasma clean.

For step 13, the bonding BCB needs to be cleared to make TPVs. This uses a similar etch process as in step 12. Here, the bonding BCB thickness below the p-contact and n-contact is around 2-2.5 µm and 3.5-4 µm, respectively. To clear both pads at the same time, optical resist is favorable compared to PMMA used for EBL. This is because the etch selectivity of AZ9260 to BCB in the aforementioned recipe is 1:1, while the selectivity of PMMA to BCB is higher than 2.5:1. So this step requires around 5µm of AZ9260, or more than 12µm of PMMA. The latter is not easily possible in EBL because of the significant charging unless it is divided into several lithography steps.

Step 14 is the final metallization using plated Au. It starts with e-beam evaporation of a Ti/Au 10/100nm seed layer at a 45° angle on top of the entire wafer to cover all of the topographic features. The patterns where Au is plated are then defined with a lithography step. This is followed by placing the sample in the 3-inch holder of the plating tool and adjusting the plating current to the open plated area to achieve a suitable growth rate. Au is then plated at a rate of 50-100nm/min depending on the Au

electrolyte concentration in the solution. After verifying the plated thickness using profilometry, the resist is removed in Acetone and IPA. The seed layer is then etched in Potassium Cyanide (KCN). Next, the Ti layer also needs to be wet etched. This is realized in the basic solution di-Ammonium hydrogen phosphate $(NH_4)_2HPO_4$ for 30 sec. The process ends by inspecting the final Au thickness and its connection from the SOA to the substrate using profilometry, optical microscopy, and SEM.

5.1.2 DFB gratings and their coupling strength

SEM images in Figure 5.3.a) and b) show the diode area before and after p-mesa definition (step 10), respectively. After defining the gratings in step 8, the thickness of the SiN hard mask used to define the p-mesa near the edge of the gratings is thicker than the deposited thickness of 50nm. So by etching down the mesa, the mesa sidewall near the gratings edge inherits the grating pattern. The latter results in higher optical losses in the active section because of the additional scattering. This can be avoided by having an offset between the two lithography steps along the diode width, and accounting for the resist quality as well.

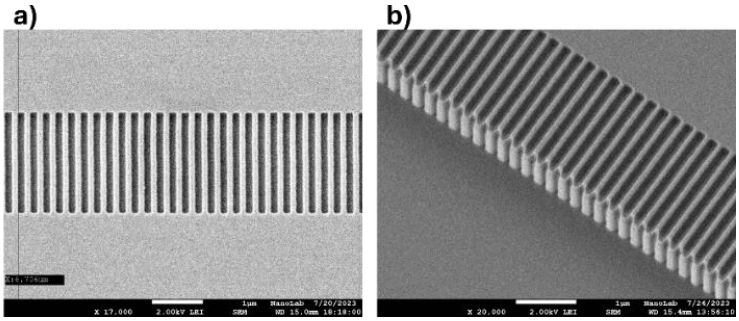

Figure 5.3 SEM image of the DFB grating: a) before p-mesa definition (step 8), b) after p-mesa definition (step 10)

Moreover, two etch depths of DFB gratings were realized to achieve suitable values of coupling coefficient (κL) for single mode operation of various DFB lengths. Shallow gratings are 120nm deep and fabricated in step 8, while deep gratings are 300nm deep and are fabricated in step 9. Note that the reported DFBs in Chapter 6 are 0.5mm-long using deep gratings and 0.75mm-long using shallow gratings. κL was previously calculated for DFBs having the same epitaxy and gratings depth [78]. Results are shown for different DFB lengths in Figure 5.4.a).

To extract the κL from measured lasers in Chapter 6, the LIV characteristics of the DFBs were analyzed at the subthreshold regime using the parameter extraction module of LaserMatrix software by Richard Schatz from the Royal Institute of Technology. An example fit is shown in Figure 5.4.b). Based on the measured ASE spectra below threshold, the coupling coefficient, the phase shift, and the parasitic reflections were determined. The DFB grating coupling coefficient κ is 48.5 cm^{-1} and 29.5 cm^{-1} for deep and shallow gratings respectively. This allows for single mode operation with kL of 2.425 and 2.213 for 0.5mm-long and 0.75mm-long DFBs, respectively. Additionally, relative to the designed DFB phase shift of 90°, the extracted effective phase shifts were 90.2° for 0.5mm DFBs and 95.6° for 0.75mm DFBs. The value of the latter is highly likely because of longitudinal spectral hole burning. Here, the carriers are depleted locally

near the phase shift via stimulated recombination, resulting in a higher refractive index. Finally, residual reflections from the end of the laser to the center of the GCs were measured between 0.1% and 1.5% varying from different samples, while the reflections from the active-passive tapers were negligible.

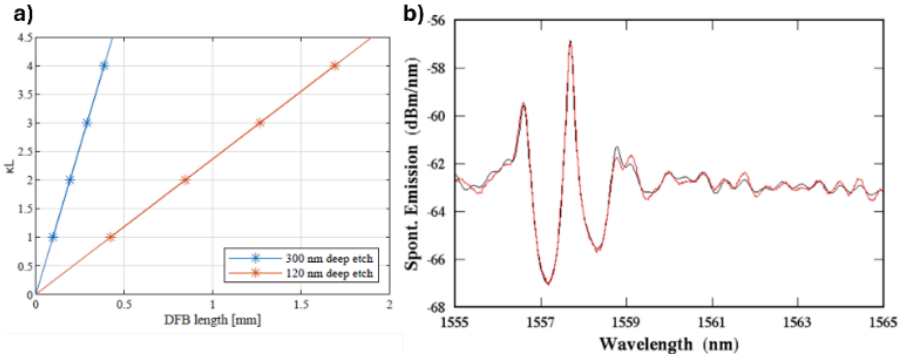

Figure 5.4 a) Calculated κL for DFB lasers with deep and shallow etch gratings (taken from [78]), b) Measured subthreshold peak (red) and its fit (black) from the 0.5mm shunted DFB at 8mA (realized by Richard Schatz from KTH).

The change of bonding BCB thickness, for instance for 3D integration, may alter the effective index contrast of the DFB gratings, which in turn could influence κL and the bandwidth of the reflection spectrum. To assess this effect, the effective refractive index of the mode (n_{eff}) in the shallow-etched section was simulated for four BCB thicknesses, 100nm, 1 μm, 2 μm, and 10 μm. The effective index n_{eff} for these BCB thicknesses is identical with a value of 3.241. The latter confirms that identical performance of the gratings is achieved for a high range of BCB thicknesses. The reason is because the mode is highly confined in the active region that is 800nm above where the bonding BCB starts, so the effect of the latter is minimal.

5.1.3 Optical losses of passive sections and the twin-guide taper

Analysis of passive losses and active-passive transmission losses of the SOA tapers is important to determine the energy efficiency of SOA-based devices. Passive devices were measured based on the transmission method using a tunable C-band laser at a power of 0dBm. Results are shown next.

The active-passive transition vertically guides light generated in the active section to the passive waveguide [157]. It includes a double-stage twin-guide taper for efficient evanescent coupling in the vertical direction between the SOA and the passive waveguide while ensuring low reflections and good coupling efficiency. An image of the taper before bonding is shown in Figure 5.5.a). The first taper section in green is not electrically pumped, so it can introduce additional losses as it contains the active material. These losses were measured using structures shown in the inset of Figure 5.5.b). Here, multiple active-passive transitions are butt-coupled in 1,2,3, and 4 pairs. The transmission losses for each structure are then measured. By linearly fitting the losses *vs* number of tapers for each wavelength, the slope corresponds to the taper loss and the y-intercept corresponds to the average GC loss. Plots for the taper loss *vs* wavelength and GC loss *vs* wavelength are shown in Figure 5.5.c) and Figure 5.5.d) respectively. It can be seen that the taper is lossy for wavelengths below 1530nm with

losses up to 4dB/taper for 1485nm. The losses between 1530nm and 1575nm however are around 1.35dB/taper. The average loss of a single GC is around 6dB for wavelengths in the range of 1500nm to 1540nm while it goes up to 9dB for higher wavelengths up to 1575nm. However, the I/O GC loss is better calibrated for in Chapter 6 by using simple GC-waveguide-GC structures placed near the active device to be measured.

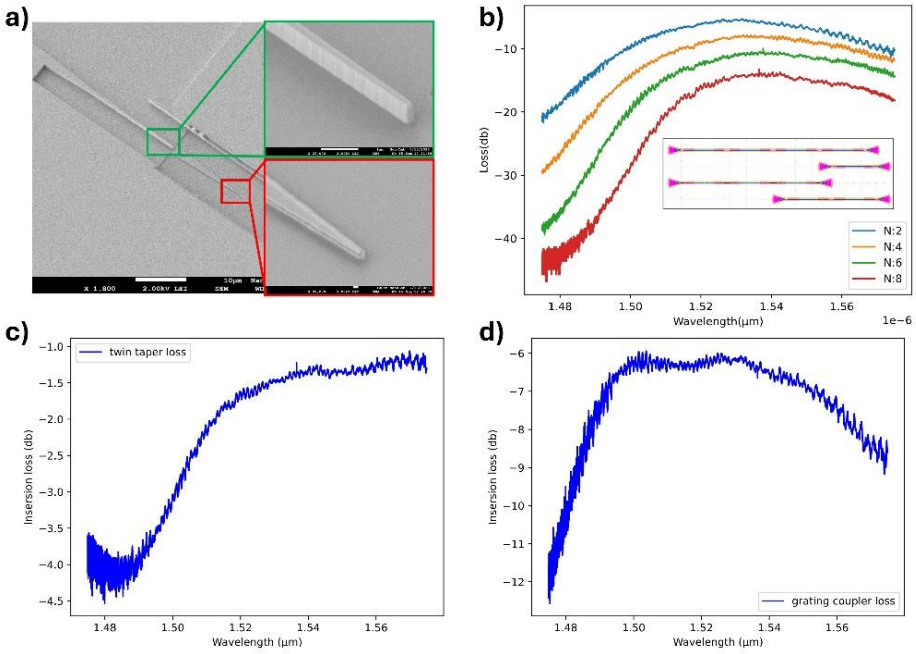

Figure 5.5 SEM image of the active passive transition, the insets are zoomed-up images of the shown regions. b) Transmission spectra through the structures shown in the inset for different number of tapers. Inset: GDS image of the measured structure. Extracted loss of c) active passive transition, d) I/O GC

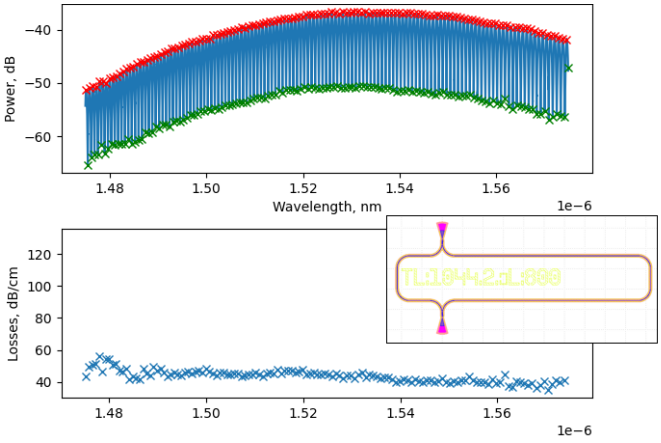

Figure 5.6 (top) Transmission spectrum through the imbalanced MZI for waveguide loss measurement, (bottom) waveguide losses per centimeter *vs* wavelength. Inset: GDS image of the measured structure

The waveguide loss was measured using an imbalanced Mach-Zender-interferometer (MZI) shown in the inset of Figure 5.6. The full theory behind this method can be found in [158]. The transmission spectrum through the MZI and extracted losses are shown in Figure 5.6. The losses were deduced by analyzing the peaks and valleys in the spectrum. Here an average loss of 40dB/cm was measured for the fabrication run of shunted C-band MQW lasers. This is related to a degraded resist that was used to define waveguides.

5.2 Design and fabrication of thermally shunted UTC-PDs on IMOS

Cross-sectional schematics after key UTC-PD processing steps are shown in Figure 5.1. Full explanations on the epi-stack shown in Figure 5.1.a) and in [105]. Most importantly, the top p-InGaAs layer act both as absorption layer and p-contact layer, the i-InP is the passive waveguiding layer, and the n-InP is the n-contact layer. Optical coupling between the PD and the passive waveguide is realized through butt-coupling. This results from the high optical confinement in the passive waveguiding layer and the high index mismatch between the absorption layer and waveguiding layer, resulting in an abrupt interface similar to a butt joint.

The fabrication flow is similar to the process realized in [105]. Hence, similar to the previous section, the common steps are discussed briefly while modifications and their reasons are given in detail. For the pre-bond steps, the PD area is first defined by removing the p-doped layers in step 2 and depositing the p-contact metal in step 3. The substrate is then bonded onto an extremely high resistivity Si substrate (> 20.000 Ω.cm) to avoid creating a short path between the n-shunt and p-shunt, and to ensure high RF performance. The etch stop layer is then removed in step 4. Next, n-contacts metallization is realized in step 5, followed by the definition of the diode mesa by removing the n-semiconductor in step 6. Note that no post-bond rapid thermal annealing (RTA) is necessary to functionalize n-contacts, so these are fully compatible with 3D co-integration with InP EICs. The I/O GC gratings and passive waveguides are then defined in step 7 and 8, respectively. Next, all semiconductor layers are removed from the GSG pad region in step 9 to reduce the RF losses [45]. The diode p-contacts are then accessed by removing the top semiconductor in step 10. Next, step 11 corresponds to BCB planarization and opening to planarize the diode topography. This is followed by step 12 where the bonding BCB is opened in the GSG pad region to create thermal shunts, and then thick Au is plated in step 13.

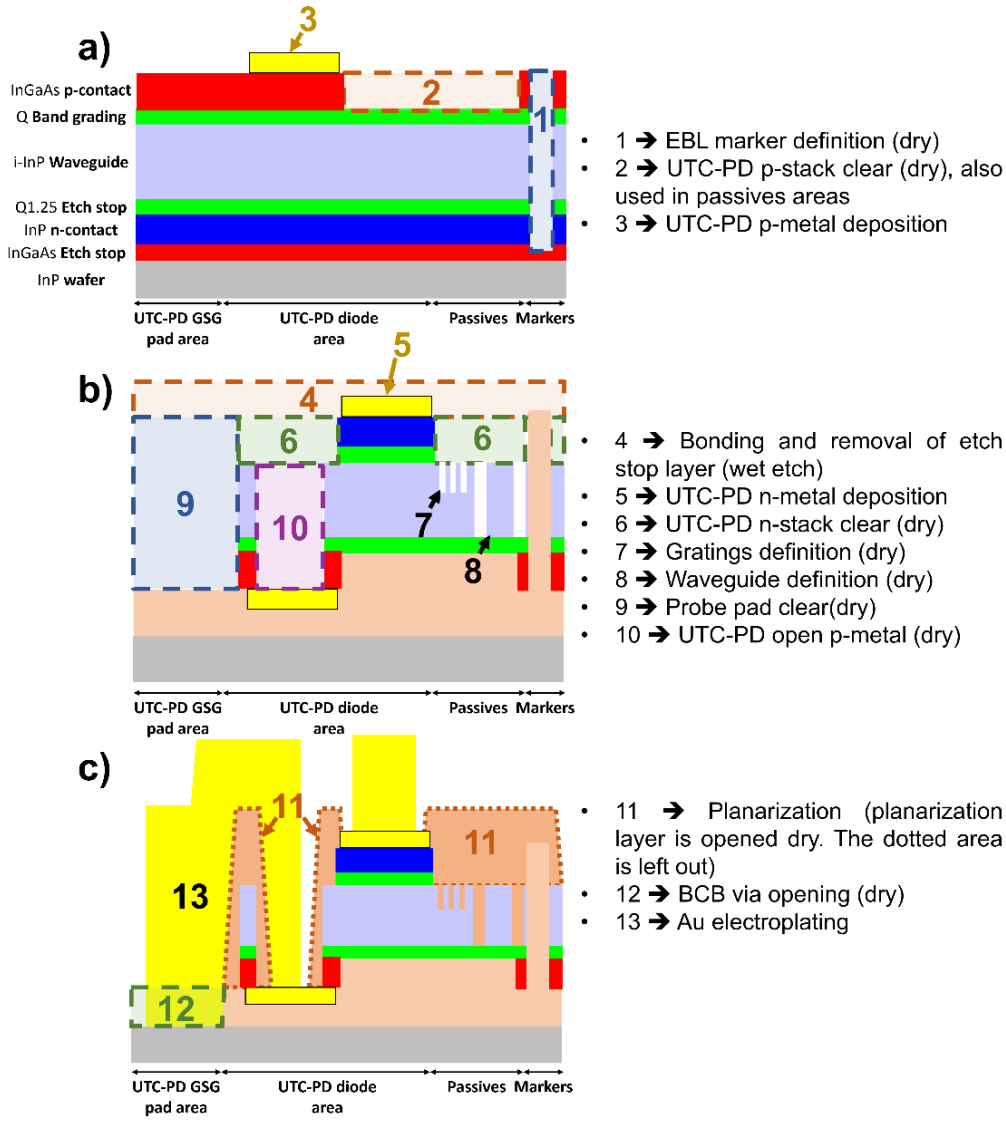

Figure 5.7 Schematics illustrating the key fabrication stages of thermally shunted UTC-PDs (dashed lines represent etched areas). a) right before bonding, b) after bonding and actives/passives definition and metal open. c) after TPV open and plating (final structure). Note that the n-contact is also shunted to Si

The thermal shunt replaces the final 200nm Au contact metallization used for standard UTC-PDs. Hence, the design mostly focuses on achieving 50 Ω impedance for these GSG pads with thick Au. Thus, the final pad dimensions are slightly different for devices with 200 nm Au metallization, 3µm metallization on top of BCB, and 3µm metallization with a shunt to Si, similar to what was discussed in Chapter 2 on CPW lines.

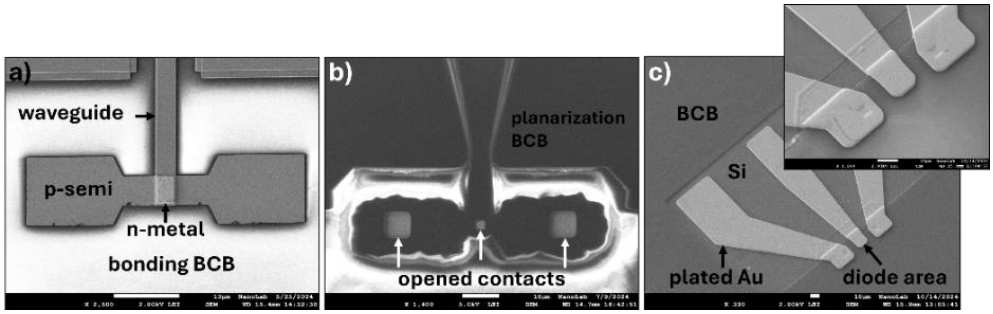

Figure 5.8 SEM images of a shunted UTC-PD: a) after waveguide definition (step 8), b) after BCB planarization and contacts opening (step 11), c) after BCB etching and Au electroplating (step 13)

Figure 5.8 shows SEM images of several crucial steps in the fabrication of shunted UTC-PDs. In Figure 5.8.a), the PD island is shown after waveguide definition in step 8. Two p-semiconductor contacts extend laterally for this GSG configuration, and the waveguide is connected to the PD. In Figure 5.8.b), the structure is planarized with BCB, which is opened near the metal contact in step 11. Finally, Figure 5.8.c) shows an image of the final structure (after step 13) with an inset zooming into the PD area. Here, the bonding BCB is opened, and 3-3.4μm of Au is electroplated to connect the diode core to the Si substrate.

Similar to what has been discussed in Section 5.1.1, the planarization in step 11 is realized with BCB for compatibility with InP EICs. Note that steps 11-13 are realized with EBL using PMMA instead of optical lithography used in DFB fabrication (Section 5.1.1). The goal is to allow for better control on critical dimensions. This is possible because the planarization and bonding BCB thicknesses are both 1μm, so these can be cleared with thin PMMA (<2μm). Also note that electroplating of high-aspect-ratio structures with PMMA has been reported [159]. Using a thin Chromium layer on top of Au could promotes better PMMA adhesion for plating compared to adhesion to Au [160]. However, this was not needed for our devices.

5.3 On-chip resistors

The on-chip membrane resistors used in this work are based on an isolated semiconductor mesa (island) with two metal connections at either end [161]. These are fabricated with UTC-PDs and used in Chapter 8 for the receiver E-PIC SoC. A schematic cross-section and GDS design of the resistor compatible with the UTC-PD processing is shown in Figure 5.9.a. The n-semiconductor layer was chosen for the resistor island as it meets the following considerations. First, the size of the resistor needs to be compact. This is because it is inserted between the UTC-PD and EIC driver input as discussed in Chapter 8. Thus, a more compact design allows for smaller RF interconnect for the E-PIC. Details on the resistor geometry follow. First, the resistor width mainly depends on the sheet resistance (R_{sq}) for a fixed resitance. The measured out-of-fab R_{sq} for the p-semiconductor is around 1000 Ω/sq, while it is around 250 Ω/sq for the n-semiconductor. Thus, using n-semiconductor layer results in 4× smaller resistors. Secondly, the resistor needs to be thermally stable for highest temperature used in the full fabrication flow, *i.e.*, no degradation in resistance after processing. In the case of integration with electronics, this temperature is 240 °C.

The following common steps are required to fabricate the resistors based on the UTC-PD process flow shown in Figure 5.7. First, the p-semiconductor is removed in step 2. The contact metal is made in step 5 and the n-InP island is made in step 6. Next, BCB is used for planarization in step 11, and the resistor contacts are reached by plated metal in step 13.

After fabrication, the resistors were measured using a 2-probe I-V setup. The measurements were carried out both directly after metal lift-off and also after thermal processing used for post-bonding steps like BCB planarization. Note that no metal spiking was witnessed at this temperature, which is well known for these Ni/Ge/Au-based n-contacts treated at temperatures above 250°C [105]. The extracted resistance after thermal treatment was compared to the designed values as shown in Figure 5.9.b). The probes resistance has an average value of 2 Ω and was subtracted, while the small metal-semiconductor contact resistance is part of the design. Here, the extracted resistance values match well with the designed resistance and follow a linear trend.

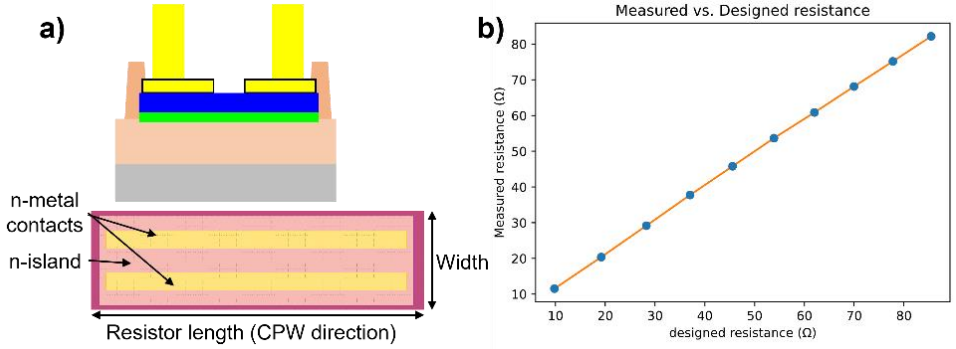

Figure 5.9 a) Schematic cross-section (top) and GDS design (bottom) of the resistor (The GDS omits plated CPW lines for visibility), b) Measured resistance at room temperature *vs* designed resistance

5.3.1 New design for pre-bond and post-bond CTLM measurements

The sheet resistance used to design on-chip resistors can be calculated using the layer thickness, doping level, and carrier mobility. However, uncertainties in doping level and carrier mobilities between the design and fabricated stack can have a significant impact on the designed resistance value. Moreover, during some processing steps, these doped layers can undergo changes that significantly affect R_{sq}, and consequently deviate the measured resistance from design by more than 100% [161]. For instance, RTA leads to the diffusion of Au into the doped layer, which creates an intermetallic region with low R_{sq}, while the doped region reduces in thickness so the total R_{sq} increases significantly [105]. Another approach is to measure R_{sq} after all the processing is done, then design resistors or other devices based on the measured value. For this, a new design of Circular Transmission Line Model (CTLM) designs are used to accurately assess the sheet resistance and contact resistance for metal-semiconductor contacts. The method details are explained in [162].

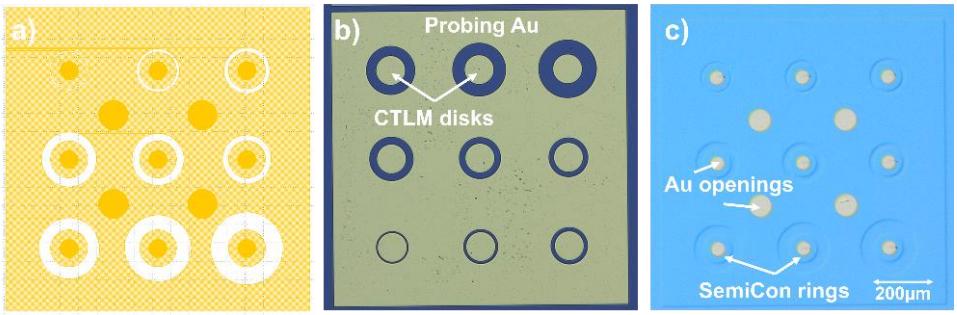

Figure 5.10 CTLM structure of an n-contact: a) GDS. Microscope images: b) before bonding, c) after bonding using polarized light

For CTLM devices fabricated before bonding, these can be probed directly and measured after metal deposition or RTA. But after bonding, these are buried underneath the semiconductor layers. To access them, CTLMs measurable after bonding were designed as shown in Figure 5.10.a). Figure 5.10.b) and Figure 5.10.c) are microscope images of the devices before and after bonding, respectively. Here, the CTLM metal discs have a diameter of 100 µm, and after bonding, the semiconductor is opened with disks having a diameter of 50 µm inside the metal disks. The opening is realized via dry etching and avoids damaging the metals. This leaves a metal-semiconductor ring with width of 25 µm, which does not affect current injection/crowding since the transfer length (L_t) is below 10µm for functional devices [163]. This allows for accurately assessing and comparing pre-bond and post-bond R_{sq} and specific contact resistance (ρ). The measured R_{sq} values before and after bonding for n-contacts from the MQW laser run used in Chapter 6 are 85 Ω/sq and 79 Ω/sq, respectively. The measured ρ before and after bonding is 1.68×10^{-5} Ω.cm^2 and 2.14×10^{-5} Ω.cm^2, respectively. These results signify that the bonding process does now significantly affect n-contacts.

5.4 Conclusions

This chapter outlined the design and fabrication process for thermally shunted SOA/DFBs and UTC-PDs, addressing the critical thermal and optical challenges associated with 3D integration. Efficient heat dissipation is achieved by implementing double thermal shunts and thick Au contacts on SOAs/DFBs,. Measurement of the optical losses and coupling strength ensures an accurate assessment of the DFBs energy efficiency. Moreover, UTC-PDs with thermal shunts were also designed and fabricated for better power handling. Fabrication here used EBL to achieve better process tolerance for BCB opening and Au plating. The fabrication for all devices was optimized according to these tolerances, and compatibility with 3D integration was maintained. The chapter also discusses the design and fabrication of semiconductor-based membrane resistors. Devices with accurate resistance can be designed by measuring its out-of-fab performance and calibrating the design based on that.

6

Chapter 6
Thermal management for 3D integrated InP photonics

Thermal management of IMOS active devices, such as lasers and UTC-PDs is challenging as a result of the low thermal conductivity of BCB. In this chapter, I present the design, simulation, and comprehensive performance analysis of DFB lasers bonded on Si using a 2 μm-thick BCB layer, both with and without a 5 μm-thick Au thermal shunt to the substrate for enhanced thermal dissipation. Using thick shunts gives significant improvements in the LIV characteristics, energy efficiency, and thermal resistance of IMOS lasers. Furthermore, the study reveals that thermally shunted lasers are compatible with density scaling down to 10% of their original size while maintaining energy efficiency, enabling the development of smaller PICs. These lasers are also suitable for 3D co-integration with electronics, even when using thick BCB layers.

Additionally, this chapter explores the design, simulation, and characterization of UTC-PDs bonded on Si using a 1 μm-thick BCB layer, and incorporating thermal shunting and dual injection techniques. The optimized designs exhibit superior performance, including reduced dark current, enhanced responsivity, and improved power handling capabilities. RF measurements also show significant improvements in their 3 dB bandwidth, more stability at higher photocurrents, and better RF output linearity compared to reference PDs. The study also shows that these PDs are well-suited for 3D co-integration with electronics, paving the way for energy-efficient receiver E-PICs, as detailed in Chapter 8. [4]

[4] This chapter is based on the work published in J2, C2, and C4. Note that Jasper de Graaf (PhI group, TU/e) designed CPW lines and the UTC-PDs. He also provided FDTD heat source data for large-scale thermal simulations.

6.1 Introduction

In the past decade, PICs have emerged as a transformative technology, enabling high-bandwidth applications in communication [7]. For next-generation data center applications, advancements in these devices need to account for paradigm shifts, such as on-chip optical links to solve the resistive losses of electrical interconnects [164], [165], and CPO for scalable traffic growth compared with pluggable optics [166]. However, as generic InP devices approach their limitations in performance, energy efficiency, footprint, and scalability, membrane photonics could be a viable alternative [74], [167]. These can be realized by integrating both active and passive devices in native material platforms such as in the IMOS platform, or by integrating the active devices into platforms such as SiPh photonics via heterogeneous integration. While significant advancements have been made in this field, a common issue for active devices in these platforms is dissipating the heat generated in the active region to the substrate. This is because the heat needs to flow through the low thermal conductivity material used for integration, mainly silica or polymer [168]. As an example, ultra-low noise lasers with no isolator were demonstrated by directly bonding InP devices onto SiPh passive devices. However, this required around 5μm of SiO_2 for direct bonding and optical mode redistribution into low loss passive waveguides, which limited the laser's energy efficiency [19]. Micro-transfer printed InP lasers on Si with 2μm buried SiO_2 layer also suffer from low thermal dissipation, which degrades their performance [169], [170].

For bonding with SiO_2, several techniques have been investigated to effectively channel the heat towards the substrate. Bonding on high thermal conductivity Silicon-Carbide (SiC) substrate with low bonding layer thickness enabled lasers with direct modulation up to 108 GHz [86]. But the drawback is that this scheme severely narrows the scope of integration capacity by solely focusing on improving the performance of a single device in the platform. Another way is using thermal shunts from high conductivity materials such as Au This was already proven to be effective for a multitude of devices on SiO_2 such as ring lasers [168], [171], and ridge lasers [172], yielding low normalized thermal resistance in the order of 0.05 K.m/W or lower, only slightly higher than generic InP lasers [173].

For polymer bonding, BCB has a very low thermal conductivity of 0.293 W/m/K, an order of magnitude lower than SiO_2 used for direct bonding[74]. So heat extraction from photonic devices is difficult as the heat generated by active devices is localized by the BCB layer. As a result, very high normalized thermal resistances were reported for DFBs on top of BCB with thicknesses above 2μm (>0.2 K.m/W), and the increased temperature seriously impaired the laser performance [174]. To solve this, bonding with low-thickness BCB on high thermal conductivity SiC was investigated, lowering the normalized resistance to 0.087 K.m/W [174], [175]. However, this narrows the integration scope and could also affect the efficiency of thermal tuning devices that benefit from heat isolation like ultra-compact phase shifters [77]. Bonding with thicker BCB relaxes the surface topology tolerances and provides a unique fabrication opportunity to seamlessly join devices from multiple material systems, such as 3D integration with electronics, which require BCB thickness above 10μm for successful bonding [21], [130]. Lasers integrated on thick BCB are heat isolated and exhibit very high resistance that severely hinders their functionality (>0.5 K.m/W) [21]. In this case,

thermal shunts could be a viable solution to channel the heat both for thin and thick BCB.

Additionally, membrane nanophotonics offer an order of magnitude scalability in terms of energy reduction and footprint relative to their generic equivalents [7], [71], aligning with their cost scalability and the stringent form factor requirements of commercial devices [20]. The footprint and density of passive devices are largely controlled by the strong optical confinement granted by the high index contrast and design choice. So these devices are miniaturized with efficient optical design [69], [70]. However, most active devices occupy large areas as their miniaturization is thermally constrained, such as 200μm-wide contacts for lasers that allocate most of their space for metallization [7]. Moreover, non-functional areas where the heat propagates between DFBs and neighboring thermally-sensitive devices can be as large as 100s of μm [176], [77]. These areas need to be limited while maintaining low crosstalk to avoid detuning the functionality of neighboring devices. Thus, evaluating the impact of active devices thermal footprint on these areas is important for scalability.

In this chapter, we report on the implementation of an efficient thermal shunt for IMOS DFBs and UTC-PDs. The active stack for lasers is based on 4 InGaAsP multi-quantum-wells (MQWs) working in the C-band, which is a mature stack used in previous IMOS laser development [68], [74], but the thermal shunt described here is flexible and can cover other stacks as well, as discussed in Chapter 7. Herein, we comprehensively analyze the performance of shunted DFBs and compare it to thermally isolated devices as a reference. We also analyze if this strategy is compatible with thick BCB to enable functional devices for 3D integration with electronics. Finally, we investigate the effect of reducing the DFB contacts width on their performance, and their thermal footprint on a larger scale to minimize non-functional areas.

UTC-PDs on BCB also face similar thermal challenges. The photocurrent generated from optical injection results in Joule heating while BCB localizes the heat to a small area [79]. This is especially detrimental to sing-injection PDs due to the poor optical field distribution in the absorption layer. These factors often lead to irreversible catastrophic failure at low photocurrents [177], [178]. Previous approaches to thermal management for UTC-PDs targeted using high-conductivity substrates or reducing the BCB thickness, which showed improved thermal dissipation [178], [179]. However, these solutions are not scalable for 3D co-integration with electronics.

To address the thermal and optical injection challenges in UTC-PDs, we introduce new PDs with two thermal management schemes. The first uses the PD contact pads as thermal shunts to the substrate. The second implements dual-injection optical schemes with thick contact pads to mitigate localized heating. Both of these methods are compatible with 3D co-integration with electronics. Moreover, unlike DFB lasers where thermal shunts primarily improve heat dissipation and energy efficiency, UTC-PDs present a unique opportunity to study the interplay between thermal management and the optical field distribution, and consequently their impact on the DC and RF performance of devices. UTC-PDs are specifically designed to target very high RF performance, so they represent an ideal active device to investigate how thermal management using the discussed schemes impacts key RF metrics such as the 3dB bandwidth and RF output linearity. Hence, the thermal characteristics of these devices was comprehensively simulated, including devices on thick BCB. The fabricated devices were then analyzed in DC and RF regimes to extract key performance metrics.

This chapter is structured into several key sections. Sections 6.2 and 6.3 cover the design and simulation setup for DFB lasers and UTC-PDs, respectively. Section 6.4 covers the experimental details and setups used to measure these devices. In section 6.5, we comprehensively analyze results from shunted IMOS lasers based on light-current-voltage (LIV) characteristics, thermal resistance, 3D integration compatibility, and density scaling. Similarly, section 6.6 covers a complete analysis of DC and RF characteristics and 3D integration compatibility of IMOS UTC-PDs. Finally, the chapter is concluded in section 6.7 by providing key results.

6.2 Design and simulation setup for thermally shunted DFBs on IMOS

The fabrication flow for thermally shunted DFBs on IMOS was discussed in Chapter 5.1. The thermal shunt is designed to improve heat dissipation by creating a direct thermal pathway from the DFB active region to the Si substrate. This is achieved by introducing a thick Au layer (5 µm) that connects the DFB mesa to the substrate through a TPV etched in the bond BCB layer. The default 2D simulation setups that correspond to the exact geometry and dimensions of the shunted and reference DFBs are shown in Figure 6.1.a and .c, respectively. A zoomed-up view of the DFB core is shown in Figure 6.1.b, which matches exactly the grown epitaxial stack and geometry of the real C-band DFBs with four InGaAsP-based QWs. Here, level 0 refers to the level where the bond BCB thickness is counted.

For the default simulation setup, the semiconductor p- and n-contacts highlighted by number 4 have a width of 12 µm. The vias slope starts directly from the end of these contacts. Asides from this default configuration, all parameters numbered in the figure from 1 to 5 are varied to investigate their influence. These included Au shunt thicknesses in the range of 0.2-5 µm and BCB thicknesses in the range of 1-30 µm.

Heat transfer in these structures was modeled based on the finite element model using commercial software (COMSOL). The latter implements the law of heat transfer by Fourier in a solid medium in the static regime given as:

$$q = -\sigma . \nabla \mathrm{T} \qquad (6)$$

where q is the heat flux, σ is the spatial thermal conductivity profile, and ∇T is the temperature gradient. The used material parameters are found in Table 6.1. The junction temperature depends on the amount of generated heat and its location. Most of the heat is generated by the active mesa core as a result of Joule heating (Q=IV) [180], [181], while other effects are less pronounced in MQW-based lasers [182]. So the red region in Figure 6.1.b) that has a cross-section of 2×0.5µm^2 is set to be the Joule heat source. For the boundary conditions, a heatsinking temperature of 300K is set at the bottom of the Si substrate. The top surfaces are set to natural convective cooling in air environment at room temperature with heat transfer coefficient h=5 W/m2/K, but this contributes to less than 1% of the overall heat dissipation. The two vertical boundary conditions are set to be thermally isolating to restrict the heat to the real DFB contact width.

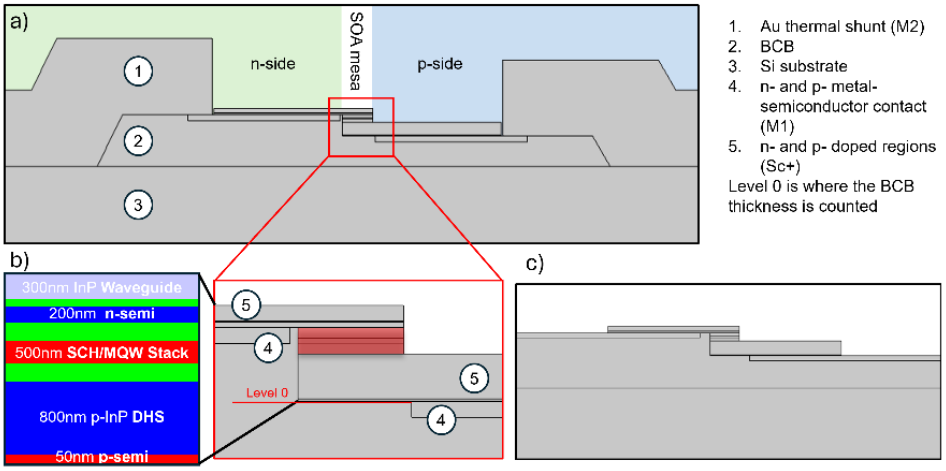

Figure 6.1 Schematic images of the simulated devices from the software for: a) shunted DFB, b) zoom-up view of the diode, c) reference DFB

Table 6.1 Thermal conductivity of materials used in the simulation

Material	Thermal conductivity k (W/m/K)
InP	68
InGaAs	16
InGaAsP	9
InGaAsP(QW)	7
Si	131
BCB	0.29
Au	316

The solution to Eq.(6) provides the full 2D thermal profile of the laser at a given power. To obtain R_{th}, the heat source power is varied, and temperature rise in the core is recorded. R_{th} is then calculated using:

$$R_{th} = \frac{\Delta T}{\Delta P_e} \tag{7}$$

where ΔT and ΔP are the temperature and electrical power differences [176]. The temperature here is the maximum temperature in the active region. We note that using the average temperature instead yields almost the same values of R_{th}. The electrical power is calculated from the thermal power as:

$$\Delta P_e = \frac{\Delta P_{th}}{(1 - WPE)} \tag{8}$$

where WPE is the wall-plug-efficiency. To accurately account for the electro-optic power conversion, we used experimental WPE values discussed in Section 6.5.1.

6.3 Design and simulation setup for UTC-PDs with better thermal management on IMOS

Standard IMOS UTC-PDs utilize 200 nm-thick Au pads on BCB, fabricated via a standard lift-off process flow. These devices are limited by heat-induced catastrophic failure at photocurrents as low as 3 mA, regardless of the PD area [79], [105], [178]. This limitation stems from the low thermal conductivity of BCB, localizing the heat to the diode region. To address this challenge while maintaining compatibility with 3D co-integration with electronics, we build on the thermal shunt concept for DFB lasers shown in Section 6.2, and propose a similar approach for UTC-PDs on IMOS. The design and simulation setup are discussed within this section, while full computational and experimental results are found in Section 6.6. To explore the effectiveness of thermal shunts, we carried out 3D thermal simulations using COMSOL, modeling heat transfer in UTC-PDs with the exact geometry and epitaxy of real devices. The simulations compared two configurations. The first is thermally isolated PDs with pads on top of BCB. The second is shunted PDs with pads connected to the Si substrate for improved thermal dissipation.

The simulation setup for reference PDs is shown in Figure 6.2. Here, the x-direction is along the PD width, the y-direction corresponds to the direction of light propagation, and the z-direction aligns with the PD epitaxy direction. The diode region consists of an isolated island where the n-semiconductor and optical coupling regions are located in the diode center and connected to the signal probe pad. Two p-contacts extend from the sides of this island in the x-direction and are connected to the ground probe pads. A GSG probe pad is used to interface the UTC-PD with RF equipment through high-speed GSG probes. For thermally isolated PDs, the pads are positioned above a 1 μm-thick BCB layer used for planarization. For shunted PDs, a BCB opening encompasses the GSG pad region. It starts 10 μm away from the diode region in the y-direction and extends to the end of the probe pads. Thus, the plated Au GSG pads connect thermally the diode to the substrate. For both configurations, the pad thickness was varied between 0.2-5 μm, and the bonding BCB thickness was varied between 1-20 μm.

Heat transfer was modeled using the material parameters found in Table 6.1. The heat source was defined in the absorption region volume having 2μm width, 130nm epi-thickness and variable lengths corresponding to PD lengths of 2.92 μm, 4.39 μm, 7.31 μm, and 10.24 μm. Note that the optical field distribution profile within the absorption region also plays a major role in heat generation. So the simulations were realized based on this exact distribution for our waveguide-coupled PDs. The heat distribution is based on the fundamental optical mode field distribution in the absorption region in the three dimensions. The latter was extracted from Finite-Difference Time-Domain (FDTD) simulations reported in [183], and is used to determine the electron-hole pair generation for the heat source term, as Joule heating is dominant [184], [185]. To detail, the field distribution is inserted in COMSOL, and the software interpolates the data into a function Q=f(x,y,z) used in the simulation. Additionally, surface boundary conditions identical to those described in section 6.2 were used here as well.

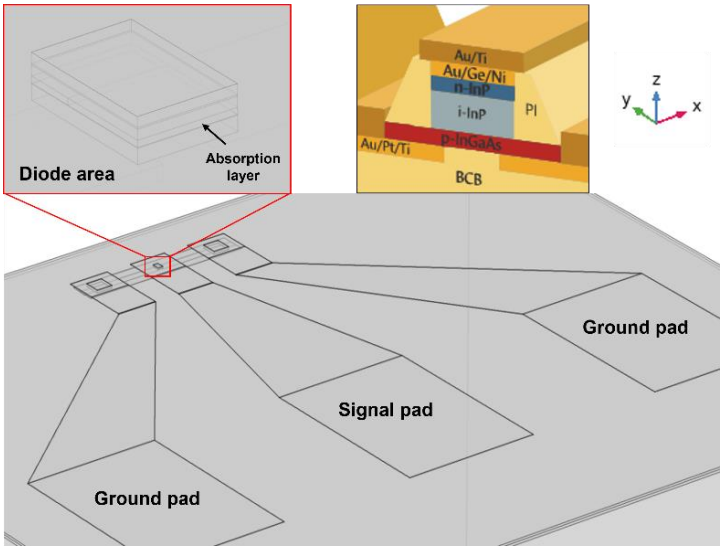

Figure 6.2: Image from the simulation setup of thermally isolated PDs, left inset: zoom into the active region, right inset: schematic image of the PD diode region matching the simulation setup, taken from [79]

The simulations were realized for single-injection UTC-PDs where light is injected from one end in the longitudinal direction (y-direction). The input optical field distribution in the absorption region as interpolated by COMSOL for the shortest and longest PDs of this type are shown in Figure 6.3. Note that the x-direction is along the PD width, the y-direction corresponds to the direction of light propagation, and the z-direction aligns with the PD epitaxy direction, same as discussed before. The dense optical field at the start of the absorption area results from the butt-coupling nature between the waveguide and PD region. Dual-injection PDs feature a more uniform distribution along the light propagation direction. However, the rapidly oscillating optical field (oscillations in the order of 100nm) results in sharp maxima and minima. These are not interpolated correctly by the tool and result in larger optical field density in the absorption region [177]. So this configuration was not simulated. Instead, a uniform power source was applied on a 4.39×2 μm^2 UTC-PD with 5 µm pad thickness to represent the ideal case. Here, the optical field is uniformly distributed in the absorption region, and hence this is considered as the best-case-scenario benchmark.

To note, we use the term baseline PDs for those having 4.39×3μm^2 dimensions and with 200nm Au and 1µm BCB. These exhibit catastrophic failure at photocurrent of 3mA based on earlier runs [178]. For other configurations, the input power is adjusted using the same profiles to reach the same temperature of thermal failure in the absorption layer. The corresponding current is then extracted. This approach allows for comparing the thermal performance of UTC-PDs for various BCB thicknesses, shunt thicknesses, and configurations (isolated *vs*. shunted), providing critical insights for 3D integration.

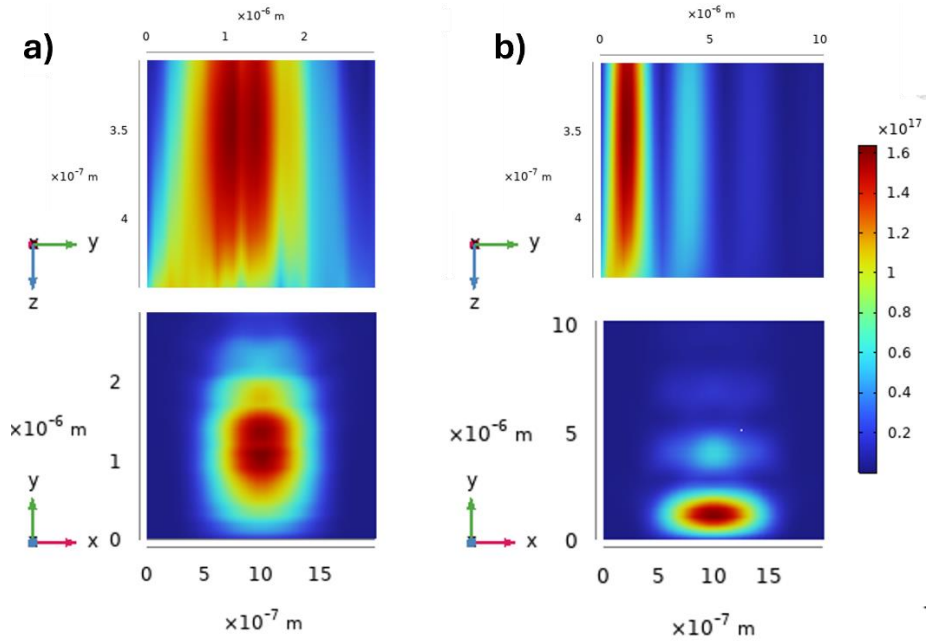

Figure 6.3: YZ-plane (top) and XY-plane (bottom) cross-sections from the input optical field distribution in the absorption region for single injection PDs with lengths of: a) 2.92 µm, b) 10.24 µm

6.4 Measurement methods

For SOAs and DFBs, the wafer was diced into 6×8 mm^2-sized chips and measured. These dimensions are used as standard dimensions for IMOS chips offered as MPW service within the JePPIX ecosystem. Measurements before and after dicing show virtually no difference in performance. The measurement setup is shown in Figure 6.4.a). The device under test (DUT) is mounted on a copper chuck having a thermistor close to it, and active temperature control is realized using a TEC, a Peltier element, and a thermal reservoir beneath it. The optical output is routed either to an optical spectrum analyzer (OSA) or power meter where we assess the DUT in direct and pulsed regimes. To accurately track the lasing wavelength peak, the OSA settings were set to -80dBm sensitivity and maximum resolution of 0.1dBm, which are the tool limits. The scan range is 10 nm around the lasing peak. For pulsed measurements, the pulse generator provides pulses of 5.6V at a rate of 100 kHz and a duration of 200ns, corresponding to around 100mA in current measured using a current probe (black circle after pulse generator in Figure 6.4.a). The OSA shows the average optical power generated by the pulses. An image of a DFB under the setup's microscope and its GDS are shown in Figure 6.4.b. Here the DFB active section is connected to the output focusing GC via an active-passive twin-guide taper followed by a 25µm of passive waveguide section.

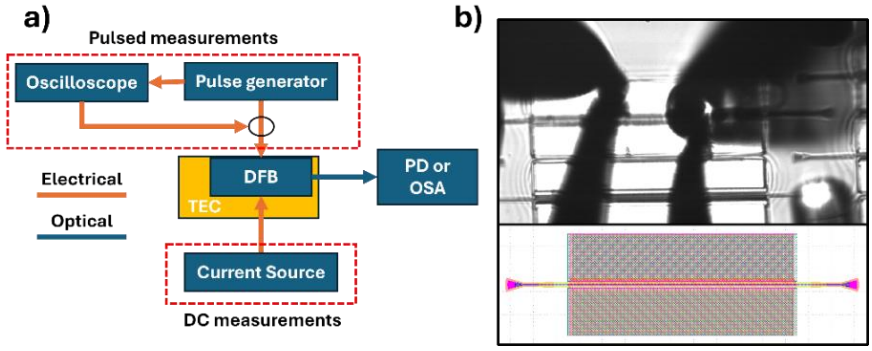

Figure 6.4 a) Setup to measure DC and pulsed characteristics of the DFB, b) 0.5mm-long DFB under the setup's microscope before the fiber is brought to the GC. Inset: GDS snapshot of the DFB.

The experimental setup used to measure DC and RF characteristics of UTC-PDs is shown in Figure 6.5. These measurements were realized on the wafer without chip singulation. For controlling the optical input power, the continuous-wave (CW) laser was fixed at a wavelength of 1550nm and power of 13dBm for DC measurements. For RF measurements, the built-in laser source of the lightwave component analyzer (shown as VNA port 1) was set to 5dBm and 1550nm. An external laser can also be used as indicated by the dotted arrow. The input optical power to the DUT is controlled by fixing the amplification of the Erbium-doped fiber amplifier (EDFA) and varying the degree of attenuation of the variable optical attenuator (VOA). The structures were measured in TE polarization. For DC measurements, the GSG probe is routed to the Keithley. For RF measurements, the UTC-PD is electrically probed with a GSG probe that is connected to a bias tee, where the DC signal is routed from the Keithley and the RF signal is routed to the VNA port 2. A 67GHz VNA is used to capture the optical-to-electrical (OE) frequency response S21 (port 1 to port 2) and S22 traces. Measurements were realized with a 2kHz filter and 801 datapoint per trace after proper de-embedding of the equipment components using standard procedures and a SOLT calibration substrate, *i.e.*, all components pertaining to the tool are de-embedded up to the GSG probe. Note that all PD measurements were done at room temperature.

To accurately calculate the external responsivity, the output power after the VOA was measured using an external power monitor. The entire optical path loss is 2.1dB. The input power into the UTC-PD was then measured based on the reading from the EDFA, attenuation in the VOA, and the path loss. In reality, this value represents the minimum external responsivity, but it is close to the real external responsivity. This is because the only difference in the optical path between the external power monitor and the on-chip UTC-PD is the additional fiber used for vertical coupling to the PD, and the latter was freshly cleaved for the measurements.

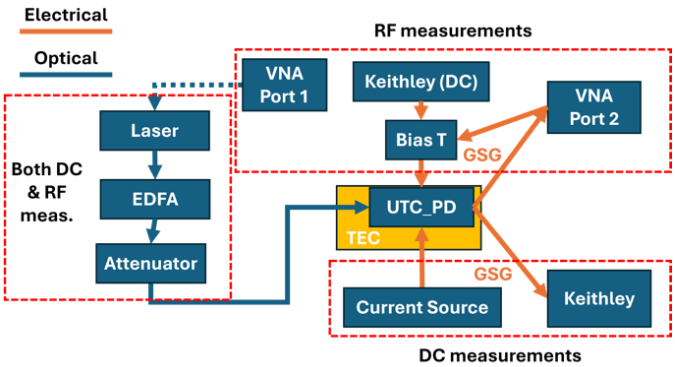

Figure 6.5 Setup to measure DC and RF characteristics of UTC-PDs

6.5 Effect of thermal shunts on the DFB laser performance

6.5.1 LIV characteristics

We measured DFBs with lengths of 0.5mm and 0.75mm. The LIV characteristics of reference and shunted 0.5mm-long DFBs are found in Figure 6.6.a). Here, the series resistances of the reference and shunted DFBs are around 11Ω and 7Ω, respectively. This is because the additional 5 µm-thick Au helps in better electrical injection into the diode. In the case of shunted devices, the metal-semiconductor overlap is 6µm while the electrical transfer length is below 2µm both for p- and n-contacts, so efficient current injection is achieved. We note that higher overlap values do not improve the performance (see Annex B).

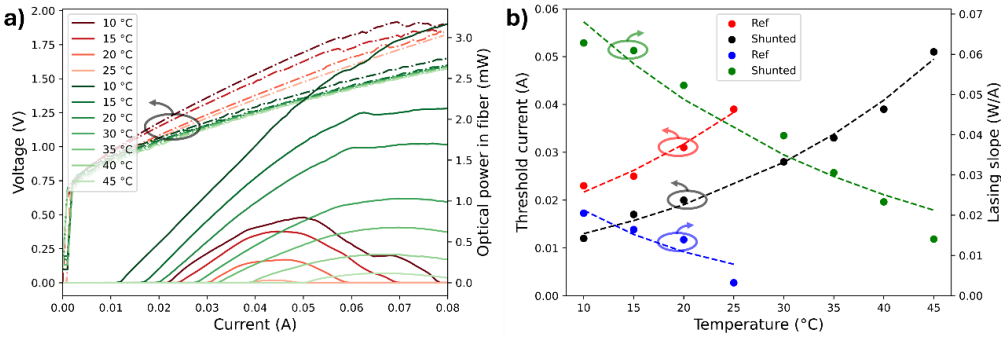

Figure 6.6 a) Light-current (solid) and current-voltage (dash-dotted) curves of 0.5mm-long DFBs. Red curves are reference DFB, green curves are DFBs with thermal shunt. b) Threshold current and lasing slope (dots) and their fit (lines) for the DFBs with and without a shunt.

As for the LI characteristics (solid lines), the maximum measured optical power in the fiber for 0.5mm-long devices is around 0.8mW and 3mW for reference and shunted devices, respectively. Reference devices work up to 25°C with a thermal roll-off starting at 45mA at 10°C, while shunted DFBs lase at an earlier current and work up to 45°C.

Shunted 0.75 mm-long DFBs work up to 52.5°C. However, we noticed irreversible damage to both DFB types if they are operated at the highest possible temperature for longer time, which will be subject to further investigation. The thermal roll-off is because as the MQW temperature increases, the stimulated recombination rate decreases, and the Auger recombination increases. So the electro-optic properties of the DFB degrade. The correlation between the differential quantum efficiency η *vs* temperature and the threshold current I_{th} *vs* temperature are given by [173]:

$$I_{th}(T) = I_0 e^{T/T_0} \tag{9}$$

$$\eta_{slope}(T) = \eta_0 e^{-T/T_1} \tag{10}$$

where η_0, I_0, T_0, and T_1 are fitting parameters that describe the exponential degradation of the laser's performance. We note that T_0 and T_1 are temperatures related to the materials used, heat source location, and geometry. The threshold current and slope were extracted for both DFBs at different temperatures and fitted using Eq.(9) and Eq.(10), respectively, as shown in Figure 6.6.b). However, better fitting can be achieved if the experimental WPE is fitted instead since it includes all of the parameters mentioned above. This is done using the following equation [173]:

$$WPE(I,T) = \frac{\eta_0 e^{-T/T_1}\,(I - I_0 e^{T/T_0})}{I(V + RI)} \tag{11}$$

where R is the electrical resistance at the measurement temperature. The experimental WPE is given as follows:

$$WPE_{exp} = P_{opt}/P_{el} \tag{12}$$

Here, P_{opt} is the waveguide-coupled optical power, and P_{el} is the electrical power. The optical power needs to be compensated for the optical losses up to the active section. This includes the average losses in the lasing wavelength range of 1555-1560nm of 5.6dB loss for the GC, 1.35dB for the active-passive twin-guide transition, and 0.05dB for the short passive waveguide connecting the GC to the DFB. Details on these loss measurements are found in Chapter 5.

We fitted the experimental WPE curves before roll-off for each temperature individually and averaged the data for η_0, I_0, T_0, and T_1. Results are found in Table 6.2. The difference between maximum and minimum values is captured by the uncertainty. Values of I_0, η_0, T_0, and T_1 are compared to state-of-the-art heterogeneous lasers and generic InGaAsP QW lasers in the following paragraphs. Figure 6.7 shows the WPE and its fit for the two DFBs. Additionally, the same curves of a shunted 0.75mm-long DFB are found in Annex B. It can be seen that WPE values of 4.7% and 16% are achieved for the reference and thermally shunted 0.5mm-long DFBs. The measured WPE for both devices deviate from the simulated curve due to early thermal roll-off where it drops significantly for the reference DFB at currents larger than 40mA while it decreases for the shunted DFB beyond this current. The WPE of the 0.75mm-long shunted DFB is as high as 18% at 60mA before roll-off at 60mA, exhibiting similar thermal behavior as the 0.5mm-long DFB in view of the injected current density.

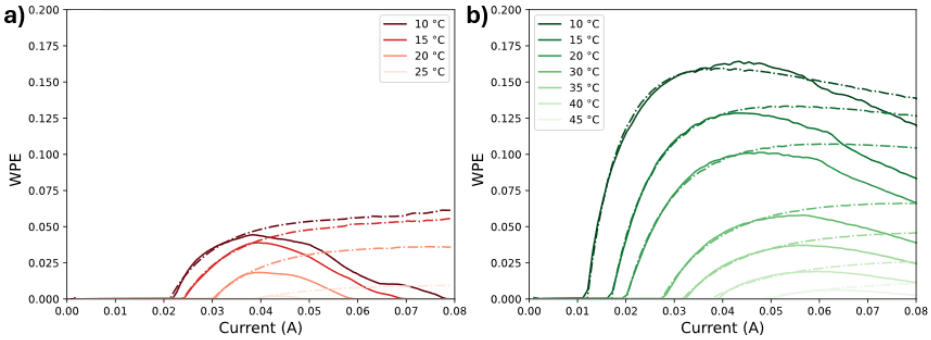

Figure 6.7 Wall plug efficiency of 0.5mm DFBs compensated for passive losses for: a) reference device, b) shunted device

The side-mode-suppression-ratio (SMSR) values are around 40dB for the reference DFB and >50dB for shunted DFBs of both lengths, with a maximum SMSR of 52.7dB at 72mA for the 0.5mm-long DFB. The SMSR values could be further improved with better cavity design involving higher κL [68]. However, these are comparable to the buried-heterostructure (BH) lasers from the generic platform using the same MQW stack [180], and also comparable to heterogeneous lasers [186]. The SMSR of shunted DFBs is better than reference DFBs because the former has a lower thermal resistance as discussed later. Compared to reference DFBs, the better thermal dissipation for shunted DFBs results in reduced thermal roll-off and wavelength shift, lower I_{th}, and higher efficiency, which all improve single-mode stability and the SMSR.

Table 6.2 Extracted parameters of the studied DFBs for different length

	SMSR	η_0 (W/A)	I_0 (mA)	T_0 (K)	T_1 (K)
0.5mm Reference DFB	40dB@ 60mA	0.21±0.09	15.35±2.35	29.28±0.82	31.58±2.72
0.5mm Shunted DFB	>50dB (60-80mA)	0.52±0.05	9.89±1.81	30.27±0.99	32.30±0.70
0.75mm Shunted DFB	>50dB (80-100mA)	0.59±0.12	11.56±0.78	29.86±1.26	32.75±1.40

I_0, η_0, and the WPE however are among the best in heterogeneously integrated lasers of similar lengths on multiple platforms [186]. The values of I_0 for the 0.5mm- and 0.75mm-long shunted DFBs are 0.989kA/cm² and 0.77kA/cm². The latter is similar to shallow-ridge (SR) generic InP lasers using the same MQW stack with I_0 of 0.62kA/cm² [180]. We note that BH generic lasers yield I_0 value of 0.35 kA/cm² because of better thermal dissipation compared to SR lasers. However, the threshold current (I_{th}) for our DFBs could be further improved by improving the DFB sidewall roughness. In this fabrication run, high roughness was verified in SEM. The latter is due to the fact that the sidewall mesa was defined after the DFB gratings, which transfers the grating pattern to the sidewall (Chapter 5).

Despite using thick BCB above 2µm, the slope efficiency for the 0.5mm-long DFB is 0.25 W/A at room temperature by accounting for the aforementioned passive losses,

which is better than BH and SR generic InP lasers [180], [181] as well as some heterogeneously integrated lasers [172], [186]. This is owed to the better optical confinement in both directions against the optical mode and confirms the energy efficiency of membrane lasers relative to their generic counterparts. The latter was also seen in O-band membrane SOAs [81]. The combination of low I_0 and good η_0 values for the shunted 0.5mm-long DFB led to WPE values as high as 16% before thermal effects start at 40 mA. This WPE value is similar to other heterogeneous lasers, as well as generic InP lasers [181], [186]. However, the thermal effects at higher currents led to rapid degradation of the DFB's performance. Here, T_0 is 13K and 21K lower than SR and BH generic lasers, indicating that the exponential degradation starts earlier. The latter is confirmed with R_{th} measurements presented in section 6.5.2.

Moreover, T_0 and T_1 are similar for the reference and shunted DFBs, indicating that the heat generation from the DFB active core itself is similar while the thermal shunt helps in efficiently directing the heat towards the Si substrate. Further improvements on the DFB structure in terms of heat dissipation are described in section 6.5.2. Moreover, to benefit from the energy efficiency of these membrane lasers, passive losses need to be reduced by using scanner lithography as discussed before.

6.5.2 Thermal resistance and 3D integration compatibility

R_{th} represents the average rise in temperature of the DFB active core volume for a given increase in dissipated power. Accurate measurement of R_{th} is realized by analyzing DFB structures as these are ideal for stable single-mode operation. Above threshold, the active region's refractive index changes with temperature but the DFB pitch is fixed, so the lasing wavelength red shifts *vs* dissipated power [176]. Hence, R_{th} can be measured by tracking the shift in the lasing wavelength of an individual longitudinal mode for different dissipated powers and temperatures [172], [187]. It is given by:

$$R_{th} = \frac{\partial \lambda}{\partial P} \Big/ \frac{\partial \lambda}{\partial T} \tag{13}$$

Here, $\frac{\partial \lambda}{\partial P}$ and $\frac{\partial \lambda}{\partial T}$ correspond to the lasing wavelength's shift *vs* dissipated power and *vs* temperature, respectively. $\frac{\partial \lambda}{\partial T}$ is used as a baseline for the shift in the lasing wavelength *vs* core temperature. For this, the DFBs were measured in pulsed wave conditions to reduce the device self-heating by current injection and allow for accurate extraction of this parameter.

The peak wavelength *vs* TEC temperature for 0.75mm-long DFBs is shown in Figure 6.8. It includes reference and shunted DFBs, as well as a DFB with a shunt only in the n-side. It can be seen in Figure 6.8.a) that the pulses are well-defined, so the wavelength shift can be tracked accurately. As a result of the linear fit, the R-squared value for all of these devices is above 0.99. The measured $\frac{\partial \lambda}{\partial T}$ is 0.0958 nm/°C, 0.0959 nm/°C, and 0.093 nm/°C for reference, n-shunted, and shunted DFBs, respectively. Hence, we choose an average value of 0.095nm/°C for all measurements, which is comparable to generic InP lasers (0.0938nm/°C) [188].

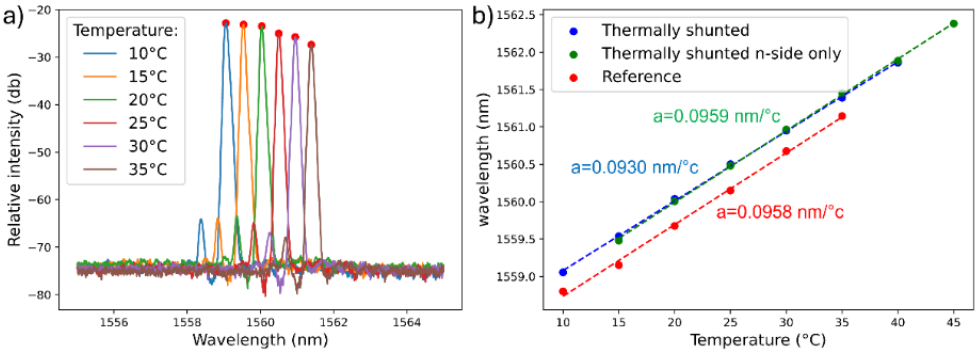

Figure 6.8 a) Optical spectra of the reference DFB *vs* TEC temperature. b) Peak wavelength of the 0.75mm-long DFBs *vs* TEC temperature in pulsed mode

Plots of the peak wavelength of 0.5mm- and 0.75mm-long, reference and shunted DFBs *vs* dissipated power is shown in Figure 6.9. Based on this, the experimental values of R_{th} for 0.5mm- and 0.75mm-long reference DFBs are 360.8±3.3 K/W and 221.6±3.6 K/W, respectively. These values for shunted DFBs of the same length are 176.0±3.0 K/W and 115.2±2.5 K/W. The simulated values for the reference DFBs with lengths of 0.5mm and 0.75mm are 338 K/W and 226 K/W, respectively. The same values for shunted DFBs of the same length are 149K/W and 100 K/W, respectively. By comparison to reference DFBs, introducing a thermal shunt using the specified geometry shown in Figure 6.1 reduced R_{th} by a factor of 2.26 from simulations, and factors of 1.92 and 2.04 from the experimental results on 0.75mm- and 0.5mm-long DFBs, respectively. We note that R_{th} for shunted DFBs is 15% higher in experiments compared to simulation. The reason is likely because of the high roughness of plated Au that indicates a lower density than bulk Au (Figure 5.1). Also, the simulation assumed an ideal boundary condition at the bottom of the Si substrate. In reality, the surface roughness of the Si substrate and the copper chuck could introduce an additional R_{th} since no thermal epoxy was used in between.

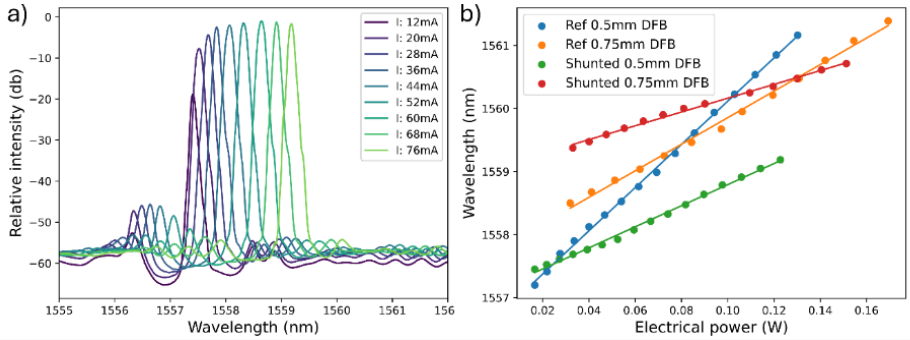

Figure 6.9 a) Spectra of the 0.5 mm-long shunted DFB. b) Peak wavelength of 0.5mm- and 0.75mm-long, reference and shunted DFBs *vs* dissipated power

Based on measurements of multiple DFBs with lengths of 0.5mm and 0.75mm, the calculated normalized thermal resistance of shunted DFBs is around 0.087 K.m/W. This value is similar to devices bonded with ultra-thin BCB on SiC [174]. But it is still higher

than state-of-the-art heterogeneous DFBs fabricated using direct bonding or die-to-die heterogeneous integration, which are in the order of 0.05 K.m/W [173]. We note that several factors need to be taken into account for accurate comparison, such as the substrate thickness, which is thinned down in other cases for better heat extraction, as well as using thermal epoxies for good attachment to the chuck. However, this difference is mostly because other methods involve bonding with SiO_2 that is an order of magnitude better at heat dissipation compared to BCB, or using ultra-thin BCB (<50nm). In our case, the BCB thickness is above 2µm, while integration with electronics requires BCB thicknesses above 10µm. So the efficiency of this shunt for higher BCB thicknesses needs to be assessed.

Moreover, further improvements on the thermal shunt could be realized by reducing the thermal dissipation path distance between the MQW core and the Si substrate as well as by bringing the shunt metal closer to the core without compromising on the optical losses [172]. we conducted more simulations with the same basic DFB structure but with these improvements on the thermal shunt. Results are found in Annex B, including the effect of wafer thinning. By reducing the total thermal dissipation path to <4µm, and thinning the substrate to around 0.2 mm, the normalized thermal resistance of these DFBs could be lowered to 0.0295 K.m/W. However, this necessitates using advanced lithography tools such as EBL for plating and BCB opening. Other improvements that necessitate new process development are explained next. The first is replacing BCB with SiO_2 via direct bonding, for better heat conductivity around the diode sidewalls [189]. Another option is using higher thermal conductivity materials to passivate the DFB sidewalls, whereby this layer acts as a direct thermal connection between the core and the thick Au shunt. For instance, Aluminum Nitride (AlN) has been shown to improve R_{th} compared to oxide claddings [190], [191]. Implementing such claddings could improve the performance similar to improvements realized with BH DFBs compared to SR DFBs in generic InP [181]. The same goes for improving the diode structure itself by implementing lateral injection devices instead of the S-shaped SOA with vertical injection, since the InP-based claddings are good for heat conduction [189]. We also note that materials and structures with better energy efficiencies are ideal for these membrane lasers working in C-band, like Aluminum-based QWs instead of InGaAsP QWs.

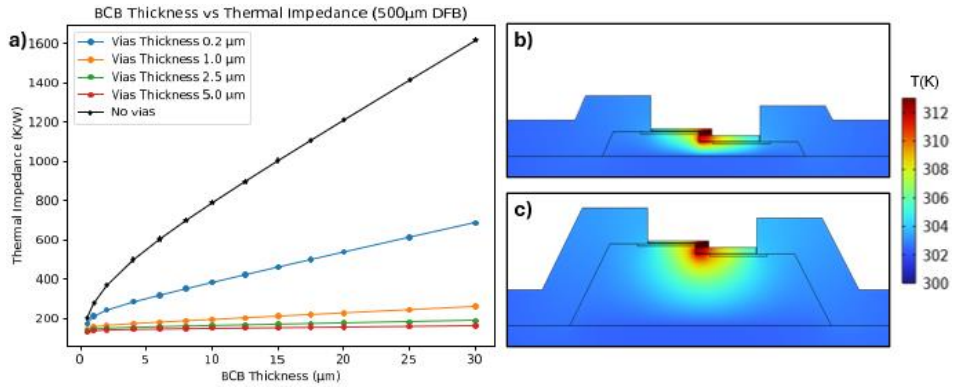

Figure 6.10 a) Simulated R_{th} for reference and shunted DFBs with various shunt thicknesses *vs* BCB thickness. Simulated 2D thermal profile of a 0.5mm-long DFB at current injection of 8kA/cm² with BCB thickness underneath of: b) 2µm, c) 10µm

As mentioned before, higher BCB thicknesses are required for void-free bonding of photonics onto electronics. However, this increases the vertical separation distance between the DFB core and the substrate connected to the TEC, so the DFB performance at these thicknesses needs to be assessed. Figure 6.10.a) shows the simulated R_{th} values for a 0.5mm-long DFB using the default geometry mentioned in section 6.2 for various BCB thicknesses and thermal shunt thicknesses. Here, we assume the same WPE as in section 6.5.1 since the energy efficiency of these DFBs at high BCB thickness is not known for other BCB thicknesses.

For reference devices, R_{th} increases linearly with BCB thickness. Here, R_{th} for the 10µm BCB required for integration of our membrane photonics with InP electronics is more than 750K/W. We note that an additional 35K/W is expected if Si is replaced with InP with the same thickness (see Annex B). Moreover, R_{th} for DFBs on 25µm BCB that is required for integration on SiGe BiCMOS electronics is around 1300K/W [21]. These would result in very strong thermal effects that strongly reduce the energy efficiency of the DFB leading to no lasing. Moreover, using thin Au for thermal shunting does not significantly reduce R_{th}, and earlier experimental trials confirmed that [157]. However, R_{th} for DFBs with 5µm-thick shunts is almost the same regardless of BCB thickness. The latter increases only slightly from 149K/W to 157K/W and 166K/W for BCB thicknesses of 2µm,10µm and 25µm, respectively. The corresponding thermal profiles to the geometries with 2µm and 10µm at 8kA/cm^2 are shown in Figure 6.10.b) and .c), respectively. Here, more than 90% of the heat is dissipated through the 5µm-thick Au shunts while the rest is dissipated downward through BCB. Consequently, a similar performance is expected for DFBs bonded using BCB thicknesses between 2µm and 30µm if a 5µm-thick Au shunt is used.

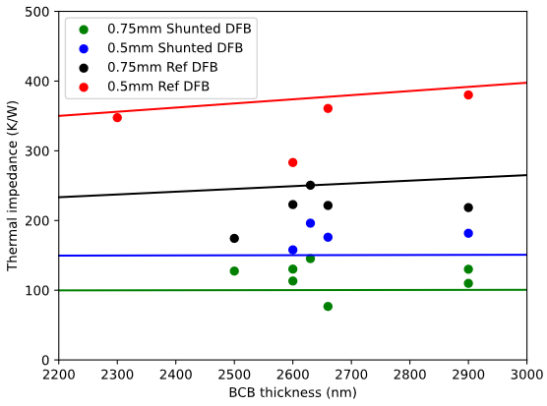

Figure 6.11 Experimental (dots) and simulated (lines) R_{th} values for different DFBs at different BCB thicknesses

Experimentally, it is not feasible to verify the performance of shunted DFBs on top of various BCB thicknesses unless several fabrication runs are realized. However, adhesive bonding with soft-baked BCB is known to result in high BCB thickness non-uniformity after bonding (Chapter 3). This accidently makes it possible to gain insights into the effect of BCB thickness on R_{th} by comparing identical DFBs from different locations on the wafer. The local BCB thickness near the analyzed devices was

measured using profilometry, where the covered range is 2.3-2.9µm. Results are shown in Figure 6.11. It can be seen that on average the shunted devices are similar in R_{th} over this range while the reference devices slightly increase in R_{th}. This can be confirmed by implementing both device types on future runs with high thickness BCB.

6.5.3 Density scaling of thermally shunted DFBs

Dense SOA arrays are essential for applications such as optical space switches and programmable photonic circuits. Increasing the array density must take into account thermal effects arising from thermal crosstalk between neighboring devices as well as efficient heat removal from the array. Figure 6.12.a) shows simulation and experimental results on R_{th} for reference and shunted devices for various DFB arrays densities, while Figure 6.12.b) compares this R_{th} to various BCB thicknesses relevant for 3D integration. We note that achieving lower DFB contact width also requires a steeper slope in the BCB opening. As seen in Figure 6.12.a), if the DFB contacts width is reduced from 200µm to 40µm, the simulated R_{th} increases by 180% and 70% for reference and shunted 0.5mm-long DFBs, respectively. Longer DFBs exhibit similar trend. However, the experimental values for 0.5mm- and 0.75mm-long shunted DFBs show no significant difference in R_{th}. This is because in the simulation we assumed perfectly isolating vertical boundary conditions, which is more relevant for the "worst-case scenario" for an array of DFBs working simultaneously [188]. However, in the experiments, we only turn on 1 DFB at a time, so the heat is better dissipated laterally across the Si. From Figure 6.12.b), increasing the array density shows an identical increase in R_{th} for all BCB thicknesses up to 20µm, suggesting that similar performance can be expected for narrow contact DFBs when integrated with electronics, hence preserving the integration density scaling. Note that the lower limit of 40µm was set based on the fabrication tolerances using optical lithography for BCB opening and Au electroplating. These tolerances can be further improved by using E-beam lithography, so the array density can be further improved.

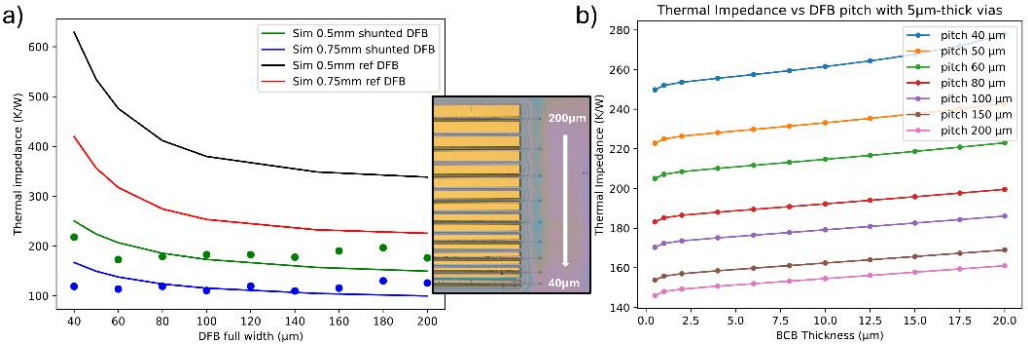

Figure 6.12 Experimental R_{th} (dots) for 0.5mm- and 0.75mm-long DFBs and simulated R_{th} (solid lines) for reference and shunted 0.5mm DFBs *vs* DFB array density. Inset: microscope image of the measured DFBs. b) simulated R_{th} for shunted DFBs with different arrays density *vs* BCB thickness

Next, we focused on studying the thermal crosstalk between the DFB and a nearby passive structure such as waveguides or ring resonators. This is because heat spreading from the DFB into these devices can thermally detune them, causing performance

degradation. For this, we compared both reference and shunted 0.5mm-long DFBs at a current injection of 8kA/cm². We used the experimental LIV characteristics for the corresponding dissipated power. The used full DFB contact width is 100µm (including both contacts), while the Si substrate and BCB extend laterally to 1000µm to study how the heat dissipates for thermal crosstalk. We also tested if the presence of semiconducting layers in open areas affects the heat spreading. We refer to these layers as cladding. This is because we use positive e-beam resists in our fabrication, so most of the semiconducting layers remain in places outside of the defined DFB areas. This included 4 simulations, for reference and shunted DFBs with and without cladding. The thermal profile of the shunted 0.5mm-long DFB without cladding is shown in Figure 6.13.a). The temperature profile was then assessed on the top surface of the BCB as this is where the photonics lie. Results are shown in Figure 6.13.b).

For reference devices, it can be seen that the temperature rise at the end of the DFB contact is as high as 13°C and 18°C for structures with and without a semiconductor layer on top of BCB, respectively. This is in agreement with the thermal profile of the DFB where the heat spreads more laterally since BCB highly insulates the heat at the top interface. However, the temperature decreases to lower than 2°C for devices with no top semiconductor at distances as low as 10µm, while this requires up to 100µm for devices with the top semiconductor remaining. The top semiconductor helps in further spreading the heat in this case.

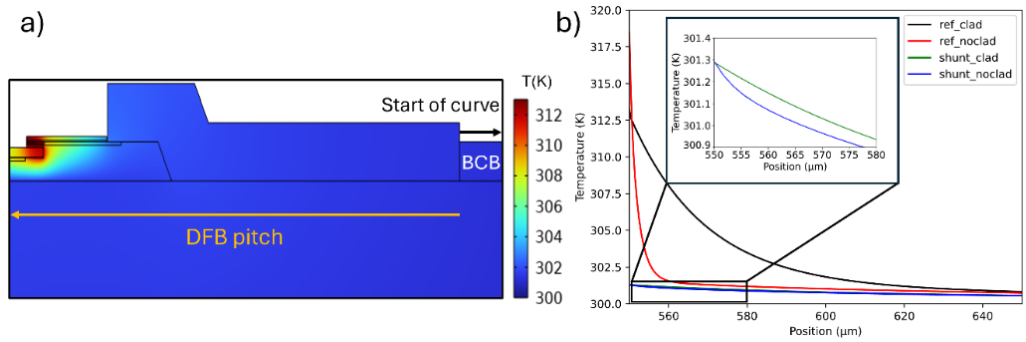

Figure 6.13 a) Thermal profile of the shunted DFB at 8kA/cm² showing where the curves in b start. b) calculated temperature rise in the passive section for the 4 configurations

For devices with a thermal shunt, the temperature rise at the end of the DFB is as low as 1.3°C for both structures with and without top semiconductor presence, indicating that lateral heat dissipation is significantly reduced for these devices. Moreover, the temperature rise is 1°C for distances around 30µm for both devices with and without top semiconductor layers. This indicates that the integration density can be maintained where thermally sensitive devices can be placed close to the DFB ridge with minimal thermal crosstalk from the DFB, even at high injection currents for the latter [42], [77]. We also note that this could be extended to devices that are in the direction of propagation of light, where thermal phase shifters or ring resonators for instance could be safely connected close to the DFBs. Moreover, lower crosstalk between photonics is expected if the BCB thickness is increased. This is because the heat spread through the substrate. Also, for higher BCB thicknesses, the separation

distance between the substrate the top BCB surface where the photonics lie increases, so less crosstalk is expected.

6.6 Effect of thermal shunts on the performance of UTC-PDs

6.6.1 Simulation results

The impact of thermal shunting for UTC-PDs was simulated based on the details provided within Section 6.3. The impact of PD length on the maximum photocurrent (I_{max}) is shown in Figure 6.14.a). It can be seen that the I_{max} is similar for all investigated PD lengths. This is because most of the optical power is absorbed within the first few 100 nanometers in single injection PDs (Figure 6.3), so the heat is generated mainly in this area regardless of the PD length. This is also referred to as front-end saturation [105]. This is evident in Figure 6.14.b, and Figure 6.14.c where the small rectangle represents the diode area while the larger rectangle is the signal metallization pad on top. Further improvements on the distribution of light could be realized with dual injection UTC-PDs [183], but this is not investigated here. However, increasing the thickness of the Au contact pad from 0.2µm to 5 µm increases the photocurrent from 3-3,4mA to 6.2-6.7 mA for the studied PD lengths. This is because the thicker Au helps in dissipating the heat outside of the small diode area.

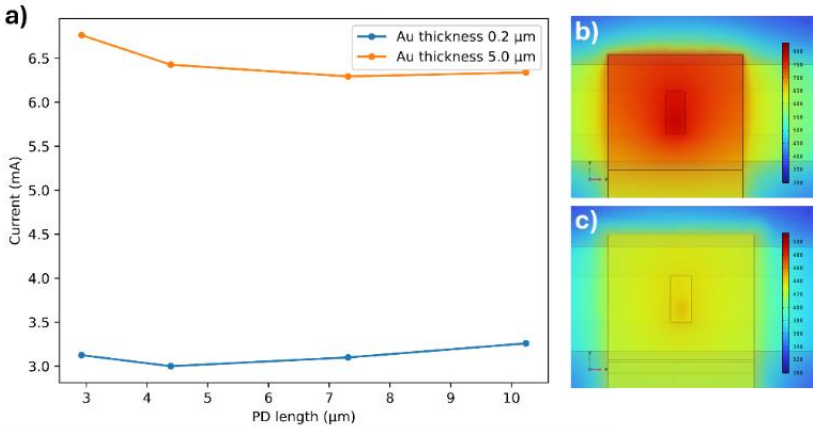

Figure 6.14: a) Influence of the PD length on I_{max} for thermally isolated PDs with two Au pad thicknesses, the BCB thickness is 1µm. Top-view thermal footprint of 4.39µm PDs at the same input power with: b) 0.2µm Au pads, c) 5µm Au pads

Moreover, we studied the impact of thermally connecting the PDs to the substrate via the Au GSG pads which act as thermal shunts. The influence of the Au thickness was simulated for values between 0.2 µm and 5 µm. Thicknesses below 0.5 µm can be fabricated via lift-off while thicker Au could be achieved via electro-plating. The studied BCB thickness is 1µm and the PD length is 4.39µm. The thermal footprint of isolated UTC-PDs with 0.2µm and 5µm Au as well as shunted UTC-PD with 5µm Au are shown in Figure 6.15 a), b) and c), respectively. Results on I_{max} *vs* pad thickness for various PD configurations are plotted in Figure 6.15.d).

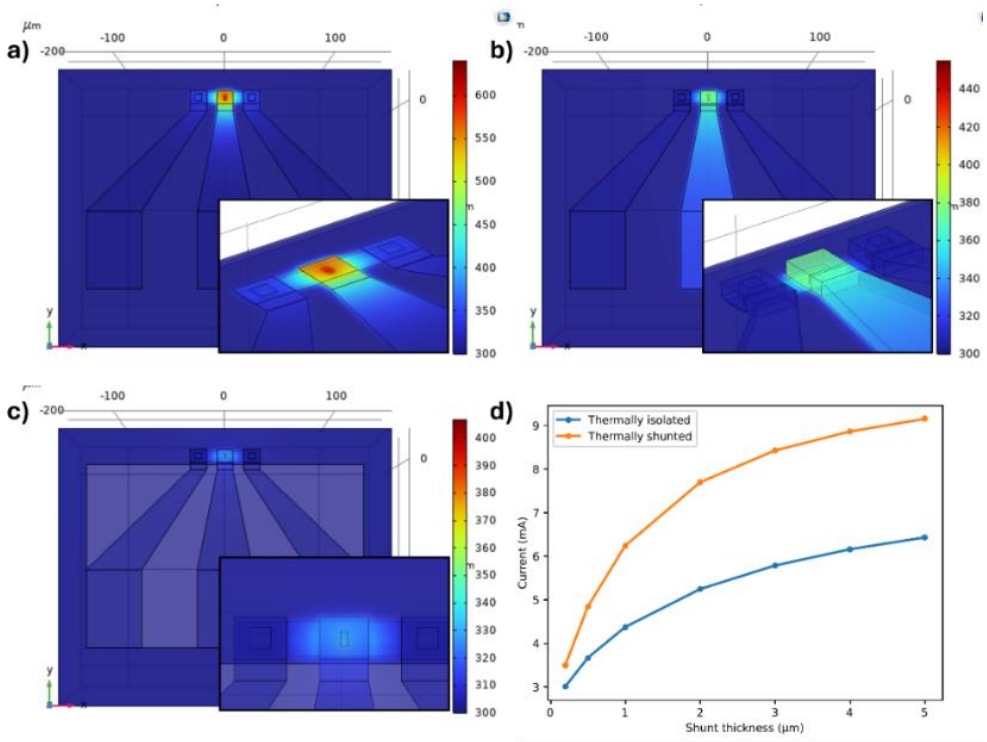

Figure 6.15: Thermal footprint of isolated PDs with a) 0.2µm Au, b) 5µm Au. c) Thermal footprint of a shunted PD with 5µm Au. d) Influence of the Au thickness on I_{max} of thermally isolated and shunted UTC-PDs

Using 5µm-thick plated Au instead of 200nm lift-off Au increases I_{max} from 3mA to 6mA for thermally isolated devices, and up to 9mA for shunted devices. However, Au thicknesses beyond 3µm are sufficient for good thermal dissipation. Moreover, from the thermal footprint figures (Figure 6.15.a-c), it can be seen that better thermal dissipation is attained in the PD region for devices with 5µm Au compared to 0.2µm Au even for thermally isolated devices. The thick Au helps in further dissipating this heat outside of the PD area, which results in further reduction in temperature. This is clearly visible in Figure 6.15.b where the temperature of the signal pad connecting directly to the PD diode is significantly higher than the two ground signals that connect to the PD contact further from the hot spot.

Figure 6.16 shows the impact of BCB thickness on I_{max} of shunted and isolated PDs with 0.2 and 5µm Au. It can be seen that I_{max} drops for higher BCB thicknesses in a similar manner for PDs with thin Au regardless of whether these are isolated or shunted. This signifies that most of the heat is still trapped within the diode area where the thin Au cannot help in further dissipating it. Using thicker Au helps in further increasing I_{max} for all BCB thicknesses. However, for these devices, higher BCB thicknesses results in further isolation of the heat in the PD area, so the current drops faster in isolated PDs compared with shunted PDs. For the latter, I_{max} is 9.15mA, 8.35mA, and around 7.5mA for BCB thicknesses of 1µm, 10µm, and beyond 20µm, respectively. Note that we also simulated direct bonding with SiO_2 using the same PD

configurations, since SiO_2 has better thermal conductivity than BCB. However, the best improvement among all configurations is below 11% improvement in I_{max}. This signifies the importance of thermal design for directly bonded heterogeneous UTC-PDs as well.

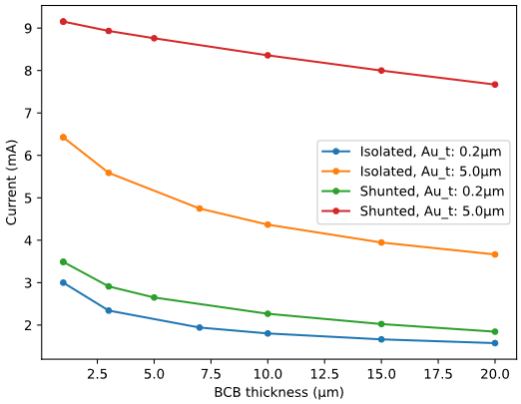

Figure 6.16: Influence of the BCB thickness on I_{max} of isolated and shunted UTC-PDs

Based on these results, considering a responsivity value of 0.7A/W and no input and passive losses, the maximum input optical power for these devices is between 7.2 and 8.1dBm, which is similar to III-V devices on the SiPh platform at an advantage of compact footprint [192]. Additionally, similar performance for standalone devices and 3D integrated devices on thick BCB is expected.

6.6.2 DC characteristics

Several device configurations were measured. We refer to single injection PDs having a metallization pad of 200 nm as baseline PDs. These PDs were not comprehensively analyzed in this run. This is because thin metallization was realized before plating. As the fabrication continued with plating afterward, the thin pads were damaged as a result of wet etching the Au seed layer. PDs with plated Au achieve pad thickness of 3-3.4μm. These consist of single injection PDs with pad on BCB (type 1), the same PDs with pad shunted to Si (type 2), and dual injection PDs with pad on BCB (type 3), as shown in Figure 6.1.a). the PD type numbers are used further in the text to avoid redundancy.

The dark I-V characteristics were measured for the 3 PD types at room temperature, results are shown in Figure 6.1.b) and .c) for two different PD areas. For PDs with a thermal shunt, the dark current at reverse bias between 0V and -3V is significantly higher than isolated PDs. This likely results from a leakage path within the GSG Au pads. It could be that during wet etching of the Au seed layer (see Chapter 5), the smooth Si surface repels the solvent more than the rough BCB, requiring higher time to leave no residues. These residues could introduce short circuit paths between the ground and signal pads on the Si side, increasing the dark current at 0V. However, for voltages between -3V and -6V, the dark current is in the same order of magnitude for all PDs. The increase in dark current for the shunted PD is much slower beyond -3V, resulting in lower dark current at -6V than the isolated type 1. This is because for these high reverse bias values, dark currents from tunneling dominate [193], which is more sensitive to the PD temperature [185], [194], [195]. The dark current at these voltage

ranges is higher for type 1 compared to type 2 and type 3. This indicates that the temperature might be lower for the latter PD types, which is confirmed with other tests on responsivity and RF performance as discussed next. To note, the dark current can be further improved by tailoring the process specifically for this purpose, for instance by implementing better passivation and low dry etch damage using a wet etch ending during the diode mesa definition [79], [194]. However, this is beyond the scope of this work.

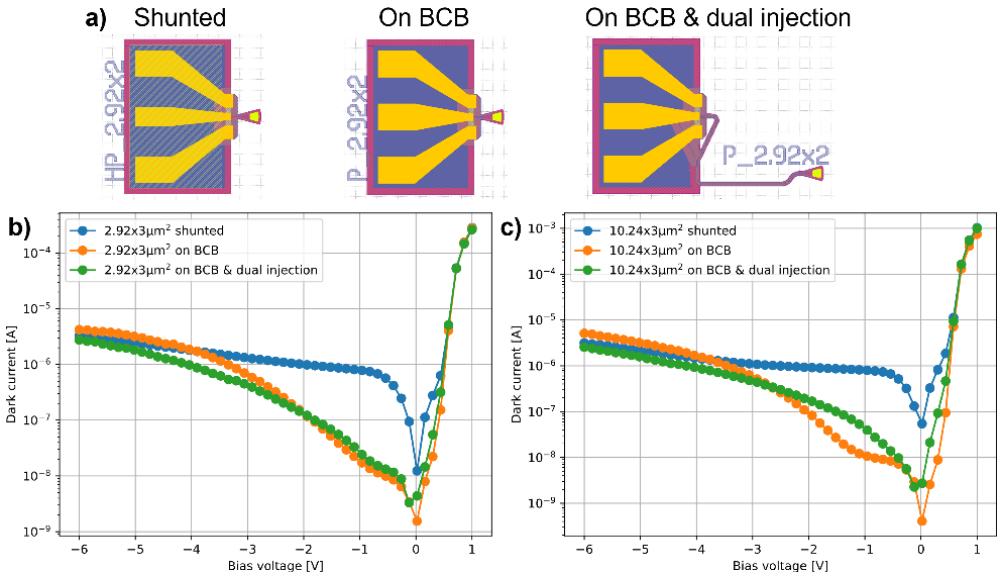

Figure 6.17 a) GDS images of the measured devices. Dark current *vs* voltage for: b) 2.92×3μm² PDs, c) 10.24×3μm² PDs

The photocurrent and maximum responsivity *vs* input optical power for 10.24×3μm² UTC-PDs is shown in Figure 6.18.a), .b), and .c), for type 2, type 3, and type 1, respectively. To measure I_{max}, some PDs were driven to catastrophic failure. Baseline PDs with thin pads from this run exhibit an I_{max} of 2.3mA, lower than the expected I_{max} of 3mA in previous runs [105], [178]. This could be related to the slightly different epitaxial stack used compared to previous runs that includes the band smoothing layers, as well as using 200nm of Au instead of 300nm for final metallization [177]. I_{max} values for UTC-PDs of type 1, type 2, and type 3 are around 3.5mA, 5.4mA, and 9.1mA, respectively. This presents an improvement of 1.52×,2.34×, and 3.95× relative to baseline PDs, respectively. The improvements expected from simulation for the same Au and BCB thicknesses are 1.92× and 2.81× for type 1 and type 2, respectively. So the experimental improvements are around 20-25% lower than expected from simulation. This could indicate that the optical field distribution in the absorption region is more abrupt than simulated. Additionally, for both single injection PD types (type 1 and 2), increasing the PD length from 2.92μm to 10.24μm does not increase I_{max} by more than 1mA. On the other hand, increasing the length from 2.92μm to 10.24μm for the dual injection PD with thick pad results in an increase of 4mA. These results confirm that the optical field distribution in the absorption region plays a major role in heat dissipation. The optimized field distribution of type 3 PDs combined with thick metallization to

extract the generated heat from the diode area improved power handling by more than 3.95×. This corresponds to a volumetric current density of 9.1/(10.24×3×0.13)= 2.27 mA/μm³. This power handling capacity of a single PD is comparable to that of to an array of 4 PDs having similar area and sharing the same CPW line for current summation. It is also comparable to dual-injection SiGe PDs on Si substrates [177].

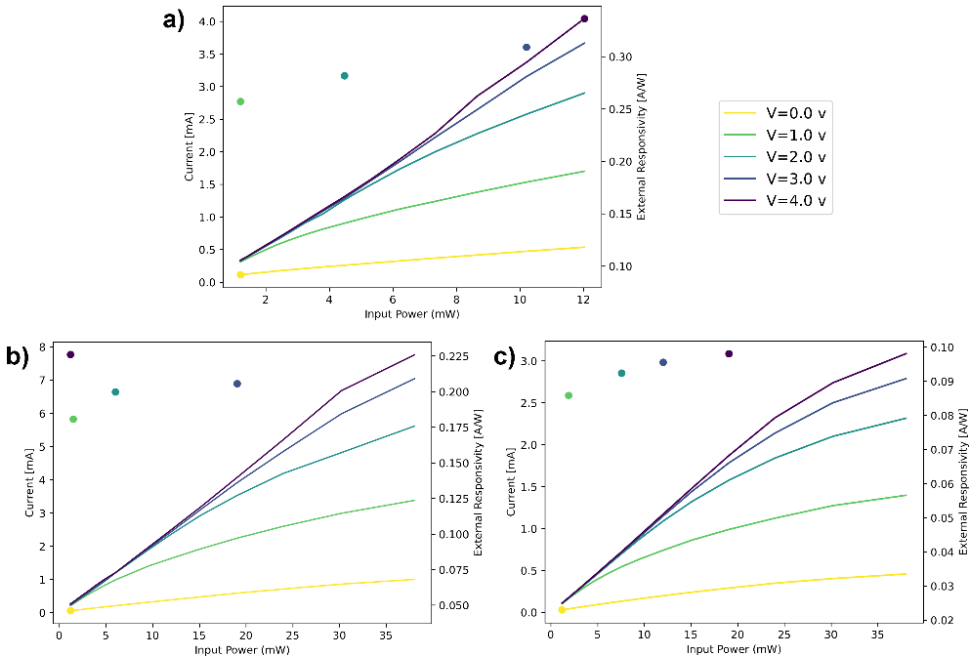

Figure 6.18 photocurrent (curve to left axis) and max responsivity for each voltage point (dots to right axis) for a 10.24×3μm² PDs: a) shunted single injection (type 2), b) on BCB & dual injection (type 3), c) on BCB, single injection (type 1)

The thermal impedance of these devices can be calculated using the following equation [27]:

$$R_{th} = \frac{T_{max} - T_{amb}}{I_{max} V_{max}} \tag{14}$$

Here, I_{max}, V_{max}, T_{max} correspond to the current, voltage, and temperature of the junction before thermal failure, respectively. T_{amb} is the ambient temperature of 20°C. T_{max} is considered as the earliest possible temperature for thermal failure, which corresponds to the n-contact metal alloy reaching its melting point of 360 °C [105], [178]. The thermal impedance of different PDs from this study is compared to PDs from the generic platform and provided in Table 6.3. Note that the reported normalized thermal impedance values may not be accurate for all device areas, especially for single injection PDs as a result of the front-end saturation. Also, this is because the thermal effects at the edges are more pronounced for PDs with smaller areas, as in the case of membrane UTC-PDs compared to generic platform PDs [185], [196]. Here, the result from the dual injection PD with thick metallization is still around 2.5× worse than that

of PDs from the generic technology and simulated large area SiPh PDs. This is because the heat generated by generic PDs is better dissipated through the substrate compared to membrane PDs.

Table 6.3 Thermal impedance of UTC-PDs on different platforms, * is a simulation result

Device	Area (μm²)	R_{th} (K/W)	Normalized R_{th} (K/W.mm²)
PD with single injection and thermal shunt with thick Au	10.24×3	15740.74	0.483556
PD with dual injection and thick Au	10.24×3	9340.659	0.286945
PD on SiPh with 100nm SiO_2 in between* [197]	100×2	550	0.11
PD from generic InP [27]	5×15	1013	0.075975
PD from generic InP [27]	5×30	844	0.1266
PD from generic InP [27]	7×25	612	0.1071

Further improvements on the optical field uniformity in the PD could lead to better power handling. This is possible for instance by implementing evanescent coupling between the PD and passive waveguide. The study this, we simulated a PD with a uniform power source in the absorption region. The performance of a 4.39×2 μm² UTC-PD with uniform power source and 5 μm pad thickness improves I_{max} up to 7.34×, *i.e.*, a maximum of 22mA could be achieved. Here, further scaling of I_{max} could then be achieved with larger PD areas as the thermal impedance of these devices scales inversely with their area [27], [185]. Finally, power handling could be further improved by designing an array of optically parallel PDs with CPW lines benefitting from the thick Au metallization and shunting near the GSG contacting area. This could further improve the optical distribution to single PDs in the array while the CPW pad dissipates the heat to increase power handling beyond 20mA [177].

In regard to responsivity calculations, devices were measured from the same cell and in a close location to avoid variability in GC losses coming from fabrication and BCB thickness non-uniformities. So the input GC losses are similar between the two single injection PD types. The dual injection PD is slightly worse than the shunted PD in terms of external responsivity because of the additional loss from the longer waveguide and the MMI (insertion loss >0.3 dB) sections, as shown in Figure 6.17.a). The highest external responsivity for the PDs from Figure 6.18 is 0.35 A/W for the type 2 PD, the 0.10A/W for type 1 PD, and the 0.23 A/W for type 3 PD. The responsivity of the single injection PD with 3μm pad on BCB (type 1) is similar to baseline PDs from previous runs having 200nm-thick pads [79], [105]. To note, the highest external responsivity was recorded for a 2.92×3μm² type 2 PD with 0.46 A/W at -4V. The reason for responsivity improvements for the two PD types compared to baseline PDs needs to be further investigated by measuring their internal responsivity. The improvement might be directly related to the diode lower temperature resulting in lower temperature gradient within the PD area. Note that temperature gradients in the diode area affects both the DC and RF performance of generic UTC-PDs, so this could be the case of membrane PDs as well [195].

6.6.3 RF characteristics

Small-signal dynamic measurements to extract the PDs OE S-parameters, using the setup shown in Figure 6.5. S21 traces were then analyzed to obtain the 3dB bandwidth at various voltages and photocurrents. The 3dB bandwidth is commonly used as performance metric for high-speed PDs. It signifies the frequency at which the output power drops by 3dB from DC (0 GHz). S21 traces of baseline PDs with thin Au was measured only for few devices to preserve the wafer before plating. Figure 6.19.a) shows the S21 traces of a baseline PD with dimensions of 2.92×3 μm² for bias voltage of -4V and various photocurrents. The traces are very similar, and the 3dB bandwidth is around 46-58GHz. Note that band-smoothing layers were designed to reduce this high voltage operation by reducing the band discontinuity between the InGaAs absorption layer to the InP drift layer, which in-turn increases thermionic emission and field emission of electrons passing through it [105]. However, these did not function properly as a result of an error in estimating the conduction band edge, so the optimal reverse bias for these PDs is at -4V. This is evident in the 3dB bandwidth results *vs* bias voltage and photocurrent, shown in Figure 6.19.b). Note that the 3dB bandwidth is determined by both the PD and the on-chip GSG probe pads. The effect of the pads could play a role here. This effect can also be de-embedded to fully isolate the UTC-PD performance. However, the 3dB bandwidth of PDs is usually reported with the effect of the pads in literature, since these are part of the DUT [79].

Results from PDs with areas of 2.92×3 μm² are shown in Figure 6.20.a) and .b) for single injection PDs of type 1 and type 2, respectively. Compared to the results from the baseline PD (Figure 6.19.b), these PDs exhibit 3 dB bandwidth exceeding 67GHz for a large range of photocurrents at -4V. Note that the value of 67GHz is the frequency limit of the VNA, and that S21 traces are captured for the same number of photocurrents for each voltage, so multiple points at -4V are overlapping at 67GHz. Similar bias dependance to baseline PDs is noted, and the bandwidth dependance on the photocurrent will be explained later on. Moreover, dual injection PDs with this small area behave similarly to single injection PDs. This is because lengths above 4 μm are required for enhancing the optical field distribution to avoid front-end current saturation [177].

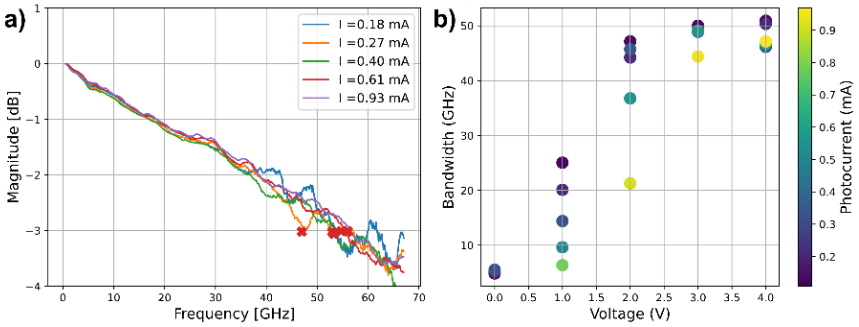

Figure 6.19 a) S21 traces of a 2.92×3 μm² baseline PD at -4V. b) 3dB bandwidth *vs* voltage and photocurrent for the same PD

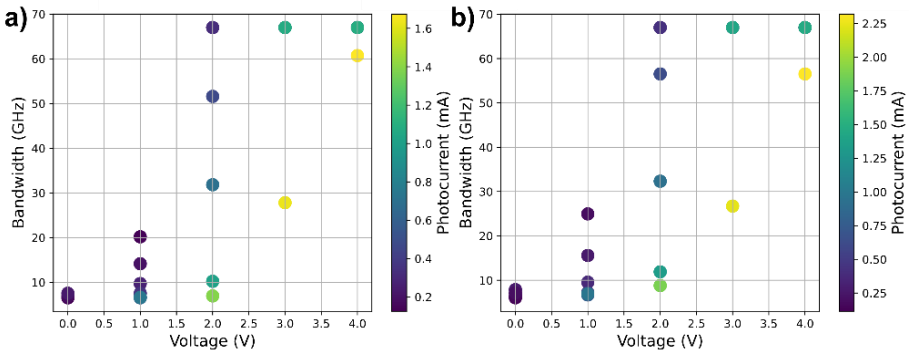

Figure 6.20 3dB bandwidth *vs* voltage and photocurrent for 2.92×3 μm² PDs of: a) type 1, b) type 2

Results from larger area (10.24×3 μm²) PDs are shown in Figure 6.21. These results show that the performance is slightly improved for single injection PDs compared to shorter PDs shown in Figure 6.20, while longer dual injection PDs significantly improved the performance, as expected from the FDTD simulations [177]. Note that the 3dB bandwidth at -4V drops below 67GHz for various photocurrents, depending on the thermal management strategy. These values are around 1.8 mA, 2.5 mA, and above 4.3mA for type 1, type 2, and type 3 PDs, respectively. These correspond to photocurrents around half of I_{max}. The type 3 PD performs better than type 2 PD, even though the latter is shunted. This is because the heat is better distributed in the PDs area for the former, so it is more efficiently extracted by the thick Au pad despite that it is not shunted to Si.

The bandwidth degradation is slightly steeper for increased photocurrents, which is related to the increasing space-charge effect from accumulated carriers [198]. However, beyond a certain current, the bandwidth degrades significantly. The 3dB bandwidth degradation as a result of increased photocurrent is steeper for PDs with smaller areas. This could be caused by multiple mechanisms. Results shown in Figure 6.20 and Figure 6.21 suggest significant degradation of the 3dB bandwidth below 67GHz happens roughly at $I_{max}/2$ and -4V. The temperature in the diode core can be calculated using Eq.(14) based on these conditions, suggesting that the temperature could reach up to 200°C in the absorption region.

Higher temperatures can reduce the efficiency of carrier collection, potentially impacting the DC responsivity of the PD. For the RF response, first note that the 3dB bandwidth of UTC-PDs depends on the RC bandwidth and transit time bandwidth. For the RC bandwidth, increased temperatures degrade the PD's RF response by decreasing the carrier mobility due to phonon scattering. This increases the effective resistivity of the semiconductor, potentially raising the series resistance. For a partially-depleted PD, temperature-induced changes in carrier concentration can alter the depletion width, potentially increasing the junction capacitance as well [199], [200]. Moreover, the transit time of electrons in the InGaAs absorption and InP electron drift layers is also affected as a result of the higher phonon scattering within the diode [201]. Additionally, high temperature gradients in the PD area caused by the concentrated generation of carriers in a small volume could exacerbate these effects [195]. Overall, further analysis is required to fully grasp the physical mechanisms behind this degradation.

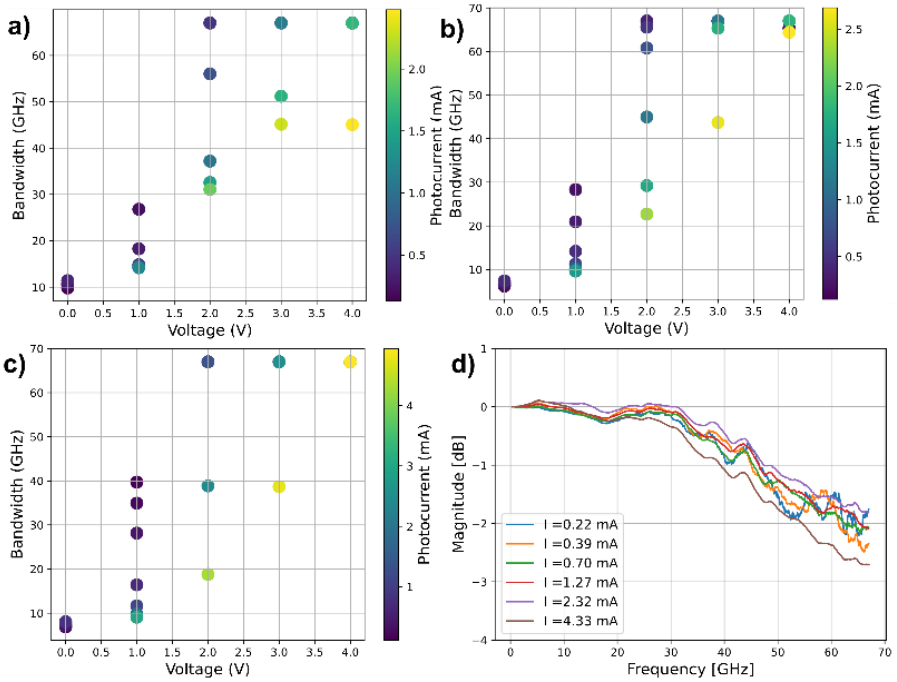

Figure 6.21 3dB bandwidth *vs* voltage and photocurrent for 10.24×3 µm² PDs of: a) type 1, b) type 2, c) type 3. d) S21 traces of the type 3 PD at -4V

Nonetheless, the combination of improved bandwidth and DC responsivity in shunted and dual injection PDs is promising for the bandwidth×efficiency product [105]. This requires further measurements with higher speed VNAs, and good calibration of the on-chip optical losses to accurately extract the internal responsivity. In addition, the best bandwidth results were achieved for a 4.39×2µm² PD having a 1dB bandwidth of 65-70 GHz, but these are not included for redundancy. Moreover, 3dB bandwidth beyond 67 GHz at photocurrent of 4.3 mA was demonstrated (Figure 6.21.d). This is the highest bandwidth×photocurrent product recorded in IMOS UTC-PDs. This current might be sufficient for low-power optical interconnects while higher powers are required for application such as mm-wave generation, necessitating adapted approaches to thermal management.

The RF power and its linearity *vs* photocurrent are also important parameters. Measuring the absolute RF power requires using a high-frequency power meter, which was not available. However, it is possible to measure the relative power from the VNA *vs* photocurrent to assess the device linearity. This was realized at a frequency of 60 GHz for the three types of fabricated PDs using thick Au. Results are shown for the three PD types in Figure 6.22.a) and .b) for PD areas of 10.24×2 µm², b) 10.24×3 µm², respectively. Since the RF output power is also dependent on voltage, only curves at -4V are shown, as this is the optimal operation condition. For PDs with width of 2µm, it can be seen that all devices are linear up to photocurrent of around 1mA. Beyond that, the two single injection PDs saturate in power while the dual injection PD continues to be linear up to 2mA. As for PDs with width of 3µm, all devices are still linear in power.

The output from the dual injection PD is still linear for photocurrents beyond 4mA, which is promising for further studies.

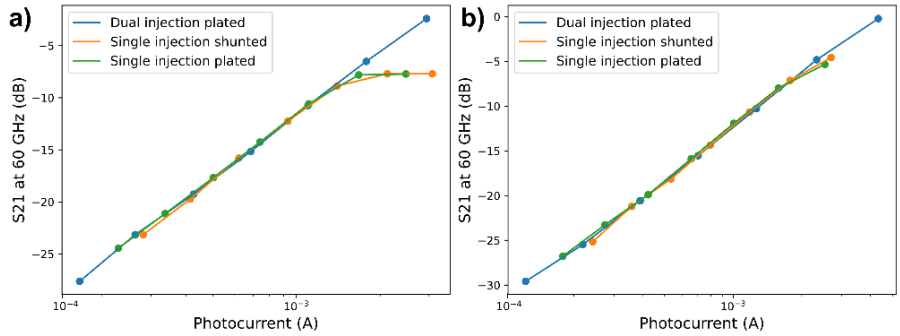

Figure 6.22 Relative output power from the VNA *vs* photocurrent at -4V for PDs with dimensions of: a) 10.24×2 µm², b) 10.24×3 µm²

For further developments on heat dissipation, the generated heat from the diode area could be better dissipated in the larger volume around it by using claddings with higher thermal conductivity such as AlN. Here, the thick Au could capture more heat and further dissipate it to the larger volume. This could be combined with thermal management strategies discussed in section 6.5, such as integrating active cooling from the top. The latter was already realized for UTC-PDs via flip chip bonding a PD to a diamond submount with high thermal conductivity, resulting in significant performance boost [202]. This also ensures that thermal management efforts are unified for lasers and PDs in the platform.

In terms of UTC-PD design, a gap between the two ground p-contacts of 1.5µm was realized for all devices. It has been shown that reducing or closing this gap enables further reduction of the series resistance and better thermal dissipation. This consequently leads to lower thermal impedance [72]. The latter requires low optical loss metals to ensure that the responsivity is preserved. As for the UTC-PD epi-stack, there are many optimizations that can be realized. These are summarized in [72], [105]. Namely, what is relevant for this thesis is reducing the operation voltage. This is done by correcting the material composition of band-smoothing layers to reduce the bandwidth-voltage and responsivity-voltage dependances.

6.7 Conclusions

In this work, we examined the thermal properties of nanophotonic membrane DFBs bonded to silicon using a 2µm BCB layer, with and without a 5µm-thick Au thermal shunt. These offer small footprint, high performance, and energy-efficient devices for 3D integration. The shunted DFBs demonstrated I_0 values as low as 0.77 kA/cm^2, and an SMSR exceeding 50 dB over a wide current range of currents. R_{th} of these devices was found to be 176 K/W and 115 K/W for 0.5mm and 0.75mm lengths, respectively. The latter is twice better than reference heat-isolated devices. This improved thermal performance is maintained across BCB thicknesses up to 30µm, indicating the suitability of these devices for scalable 3D integration with photonics on other platforms or on EICs. Moreover, we observed that the thermal resistance was consistent

across DFB array density values ranging from 40 to 200μm, with a minimal temperature rise of only 1.3°C relative to the heat sink temperature at the DFB contact end under an 8 kA/cm^2 driving current. These results underscore the potential for miniaturization of circuits with shunted nanophotonic devices.

For UTC-PDs, the dark current of shunted PDs was measured, showing a small leakage path but also an improvement due to lower thermal effects. Compared to baseline PDs, the maximum photocurrent was improved by a factor of 1.52×,2.34×, and 3.95× for type 1, type 2, and type 3 PDs, respectively. The external responsivity of shunted PDs is also improved, with a best value of 0.46 A/W at -4V for PD of 2.92×3μm^2 area. The 3dB bandwidth of devices was improved beyond 67 GHz by using thermal shunts and dual injection schemes. The RF output power linearity was also confirmed for PDs with 10.24×3 μm^2 area for currents close to $I_{max}/2$.

Chapter 7
Low Polarization Sensitive SOAs on IMOS

This chapter addresses the development of compact and low-polarization-sensitive SOAs for O-band and C-band operation on the IMOS platform. Polarization insensitivity is achieved by using a thin tensile-strained bulk active layer based on a novel stack. Hence, the design, growth, and characterization of the epi-stack is discussed. The SOA design also leverages the enhanced thermal dissipation scheme discussed in the previous chapter to preserve the energy efficiency. For O-band devices, a 0.5mm-long SOA achieves a peak gain of 11.5 dB at current density of 2.5kA/cm^2, and with minimal polarization-dependant gain (PDG) below 1 dB over a 25 nm bandwidth, from 1312 nm to 1337 nm. These characteristics make it suitable for applications where both a standalone SOA and cascaded SOAs are required, such as pre-amplification and optical switching. This also highlights the potential of O-band IMOS devices, where combining this with the potential for 3D integration could be ideal for high-density SiPs. Simulation results for C-band SOAs show PDG below 1dB across a 40 nm bandwidth for current densities in the 2-4kA/cm^2 range. Finally, we also cover the fabrication tolerances for C-band and O-band I/O GCs, as the O-band GCs were first realized within this work. [5]

7.1 Introduction

Development of PICs for data center applications revolves around several key aspects. These include polarization handling, active passive integration, component and facet insertion losses, and device footprint. SOA devices in PIC technologies enable a wide

[5] This chapter is based on the work published in J8, C7, and C12 . Note that Desalegn Feyisa (ECO, TU/e) designed the epitaxial stack, O-band active-passive taper, and O-band passive devices. He was also the main responsible for measurements while I helped in troubleshooting and discussions. René van Veldhoven (NanoLab, TU/e) carried the epitaxial growth.

range of functionalities, such as realizing on-chip lasers and signal loss compensation. Monolithic integration of these devices on native substrates provides a reliable solution for reducing facet losses and increasing the integration density, which are imperative for advanced optical applications [203]. Furthermore, co-integrating SOAs within platforms featuring high index contrast for compact passive and active devices offers large possibilities for footprint and power budget scalability. These features are possible within the IMOS platform, where active devices such as SOAs and UTC-PDs are seamlessly integrated with ultra-compact passive devices [68], [74]. Other high index platforms such as SiPh realize active-passive functionalities via heterogeneous integration, making it more difficult to have polarization insensitive (PI) SOAs in such platforms [204].

For IMOS, polarization handling devices were previously introduced in this platform, such as polarization converters and filters [78], [205]. These are compatible with the standard active stack using unstrained MQWs. However, the asymmetry of the MQW gain medium implies that realizing PI-SOAs with these devices necessitates a polarization converter and double the number of SOAs. This results in larger footprint and energy budget, higher optical losses from the added passive components, and higher fabrication complexity [78], [206], [207]. For the generic InP platform, unstrained PI-SOAs were realized based on bulk active core serving as a symmetric gain medium, both for O-band and C-band operation [208], [209]. These offer low PDG across a large input power range, high gain, and low noise, which can serve both as a booster SOA or SOAs for switching functionalities. Moreover, these devices can be fabricated using the same process flow for MQW-based devices, with minimal structural and material property changes. Hence, a similar approach is more favorable to demonstrate PI-SOAs on IMOS.

To guide the bandgap engineering approach, note that the modal gain is considered as a key metric for polarization sensitivity in semiconductor amplifiers. The latter is the product of material gain and confinement factor for the transverse electrice (TE) and transverse magnetic (TM) polarizations. For bulk SOAs, the material gain is usually symmetric for the two polarizations, while the confinement factor depends on the structure dimensions and is usually smaller for TM. To compensate for this and achieve equal modal gains for TE and TM, the material gain can be controlled via strain. Strain measures the mismatch between the in-plane lattice constant *(a)* of an epitaxially deposited layer and the substrate or layers beneath. The layer in this case is the bulk active InGaAsP core and the substrate is composed of InP. Note that TE light emanates from stimulated electron-hole (e-h) band-to-band recombination between holes in the heavy hole (HH) band and electrons in the conduction band. For TM light, the source of holes is the light hole (LH) band. For a relaxed lattice-matched layer, the energy levels of the LH and HH are identical. However, introducing strain to the epitaxial layer can alter the energy levels [210]. Tensile strain where the layer has a larger *(a)* than the substrate shifts the LH upward, resulting in higher probability for e-h recombination emanating TM light. Compressive strain shifts the LH downward, so it has the opposite effect. Hence, introducing tensile strain in the active core results in higher material gain for TM than TE, which can compensate for the difference in confinement factors to realize PI-SOAs with low PDG [211].

To note, MQW-based SOAs can also employ tensile strain for PI performance. However, these devices present problems in terms of PDG uniformity across the gain bandwidth and injection current, since these characteristics heavily influence the

material gain for that stack [212]. The strain required is also much higher than for bulk actives, which could lead to strain relaxation via defects that introduce additional optical losses and electrical leakage paths [213]. Also, for bulk active SOAs, introducing strain provides a degree of freedom that allows for achieving polarization independence while maintaining an optimal active core thickness. For comparison, square-shaped bulk active SOAs are also polarization independent since the confinement factor is the same for TE and TM, and these were demonstrated in literature [209], [214]. However, increasing the epi-thickness results in higher transparency currents and diode resistance, which are not compatible with the energy efficiency, thermal management, and integration density of membrane devices. Hence, employing thin bulk active layers with tensile strain could be a viable solution for PI active membrane devices.

This chapter revolves around modeling, design, fabrication, and characterization of O-band and C-band PI-SOAs on the IMOS platform. This functionality is realized via tensile-strained bulk InGaAsP active core as discussed earlier. The design and fabrication of these devices is similar to MQW-based SOA/DFB devices reported in Chapters 5-6, with the main difference being the epitaxial design of the active core. Hence, Section 7.2 introduces the device design, layer growth and characterization, and fabrication outcome. Section 7.3 explains the experimental setups used to measure key characteristics of these SOAs, including transparency current, net modal gain, and PDG. Section 7.4 presents key characteristics for O-band SOAs. Section 7.5 presents preliminary measurements on C-band SOAs. Additionally, 7.6 presents fabrication tolerances of I/O GCs for IMOS PICs. Finally, Section 7.7 concludes the work by providing a summary and potential improvements.

7.2 Design, growth, and characterization of the layer stack

This section details crucial steps in the design of PI-SOAs based on bulk active core. Device and epi-stack design for O-band and C-band PI-SOAs is first discussed. Compositional and structural characterization of the stack is also realized. Finally, outcome of the fabrication run is shown.

7.2.1 Layer stack design

The design and simulation of the SOA stacks is realized using HAROLD commercial software from Photon Design. The stack is based on InGaAsP-InP materials since the in-house growth of these materials is controllable and can be precisely calibrated. The complete O-band epi-stack is shown in Table 7.1. The active waveguiding core is composed of layers 7-9, with a thickness of 300nm. Layer 8 represents the active InGaAsP having a photoluminescence (PL) wavelength of 1350 nm and tensile strain of 0.18%, these values are further explained in later text. This thickness is higher than the threshold for quantum confinement to guarantee bulk behavior and achieve a sufficient optical confinement factor. It is sandwiched between two 125 nm-thick SCH layers, with bandgap wavelength of 1.05 μm. The value of the latter ensures enough band offset to layer 8 for good electrical confinement in the active region.

The active region is buried between n- and p-type layers for current injection, which are layer 10 and layers 2-6, respectively. The highly-doped p-InGaAs (layer 2) used for

p-type ohmic contact with low specific contact resistance induces high losses to wavelengths in the IR region, so it is separated from the mode propagation region by 800nm of p-InP cladding (layer 5). The latter represents a safe compromise between the diode resistance and low propagation loss, but it can be lowered to 500nm as well [157], [161]. Double heterostructure (DHS) layers 5-6 and 10 also provide optical confinement of the mode in the active waveguiding region. Additionally, layer 12 represents the 300nm InP passive waveguiding layer, where all passive functionalities are realized. Finally, layer 13 is an etch-stop layer used for removal of the InP wafer using wet etching with HCl.

For the C-band epi-stack, layers 1-6 and 10-13 are identical to the O-band stack. Layers 7 and 9 are composed of Q1.25 instead of Q1.05 to confine C-band light. The bulk active core (layer 8) composition was optimized based on this stack. It requires a PL wavelength of 1600nm and 0.23% tensile strain to achieve PI performance at 1550 at current densities in the 2-6kA/cm^2 range, as discussed later in text.

Table 7.1 Epitaxial layer stack for O-band PI-SOAs, also including the measured grown layer thicknesses. The active InGaAsP* material has 0.18% tensile strain

Layer #	Function	Material	Doping (cm^{-3})	Thickness (nm)	Meas. thickness (nm)		
					Center	Middle	Edge
1	cap layer	InP	n.i.d	50	NA	NA	NA
2	contact 3	InGaAS	p=2×10^{19}	30	50	45	37
3	contact 2	Q1.25	p=8×10^{18}	10			
4	contact 1	Q1.25	p=4×10^{18}	10			
5	DHS	InP	p=1×10^{18}	800	851	811	785
6	DHS 1	InP	p=3×10^{18}	100			
7	SCH	Q1.05	n.i.d	125	306	295	280
8	Bulk active	InGaAsP*	n.i.d	50			
9	SCH	Q1.05	n.i.d	125			
10	DHS	InP	n=4×10^{18}	80	64	61	57
11	Etch stop	Q1.25	n=1×10^{19}	20	22	21	19
12	WaveG	InP	n.i.d	300	315	300	285
13	etch stop	InGaAs	n.i.d	300	NA	NA	NA
14	substrate	InP	n=1×10^{18}	NA	NA	NA	NA

Simulations were realized on the S-shaped SOA based on this epi-stack using PICWAVE from Photon Design. The latter is used to calculate the evolution of the field propagating in the SOA through the slow-varying envelope approximation. For a 2μm-wide SOA, the extracted optical confinement factors Γ for TE and TM are 11% and 8.5%, respectively. These are comparable to IMOS SOAs with 8 MQWs [215]. The relationship between internal SOA gain, confinement factor, and material gain g_m is given as follows:

$$G = 10\,log_{10}(e^{(\Gamma g_m - \alpha)l}) \qquad (15)$$

Here, G is the internal gain and α is the material loss. The goal is to minimize PDG, which is the difference between the TE and TM internal SOA gains (G_{TE}) and (G_{TM}), respectively. These are related to the material gain and confinement factors with the relation that follow.

$$PDG = |G_{TE} - G_{TM}| = 10\, log_{10}\, e^{(1-\Gamma_{ratio} g_{ratio}) g_{TE}} \qquad (16)$$

Where Γ_{ratio} and g_{ratio} are the confinement factor ratio $\Gamma_{TM}/\ \Gamma_{TE}$ and material gain ratio g_{TM}/g_{TE}, respectively. By neglecting the polarization-dependent free carrier absorption losses, the PDG depends mainly on the confinement factor and material gain ratios [206]. An ideal PDG is close to unity, but the asymmetric waveguide structure dimensions and material gain usually result in values smaller than 1.

MQW gain structures usually exhibit high anisotropic material gain ($g_{TM}<g_{TE}$) and anisotropic confinement factor ($\Gamma_{TM}< \Gamma_{TE}$) [213], [216]. However, bulk gain structures have isotropic gain ($g_{ratio}=1$). So anisotropy in the modal gain (Γ×g) here relates mainly to the confinement factor ratio. To achieve PI modal gain for a wide range of current densities, the optimal tensile strain of the O-band active core is 0.18%. Here, the tensile strain increases the material gain for TM light, compensating for the smaller confinement factor for TM. The TE and TM modal gains in a 0.5mm long tensile-strained SOA at 4kA/cm² are shown in Figure 7.1.a), simulated in PICWAVE. Here, the PDG is close to 1 for a large wavelength range between 1270nm and 1340nm. Moreover, this low PDG is maintained across current densities between 2 and 6kA/cm².

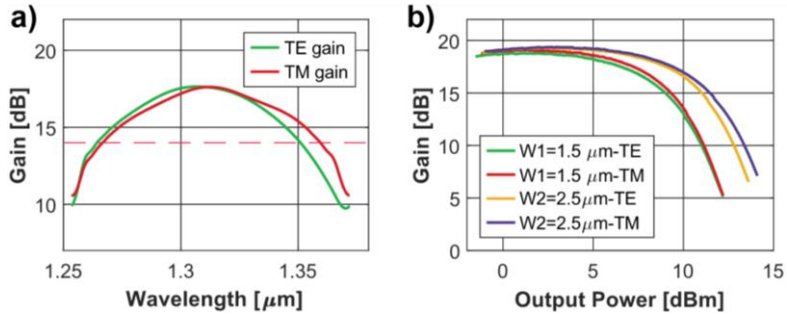

Figure 7.1 a) O-band gain versus wavelength for a 2µm-wide 0.5mm-long SOA at current density 4kA/cm². b) Net gain versus output power for 0.5mm-long SOA at 4kA/cm² simulated for widths of 1.5 µm and 2.5 µm.

The SOA width is also critical for the output saturation power of the SOA. This is because the latter depends on the effective modal cross-section A and saturation intensity I. It is given as [217], [218]:

$$P_s = C.A.I = C.\left(\frac{dw}{\Gamma}\right).\left(\frac{h\nu}{\delta\tau}\right) \qquad (17)$$

Here, C is the input coupling efficiency, d is the active layer thickness, w is the device width, h is the Planck's constant, v is the frequency, δ is differential gain, and τ is the carrier lifetime. Note that the confinement factor depends on d and w. Figure 7.1.b) shows the net TE and TM gains for various output powers in a 0.5mm-long SOA at 4kA/cm² having widths of 1.5µm and 2.5µm. The saturation power based on 1dB

compression is 8.5dBm and 11dBm for SOA widths of 1.5µm and 2.5µm, respectively. A width of 2µm was chosen as an optimal compromise between saturation power and confinement factor. This width also preserves the PDG for a wide range on input powers between -20dBm and 5dBm. Note that the same width is conventionally used for MQW-based IMOS SOAs, as discussed in Chapter 6.

The active-passive twin-guide transition between the SOA and passive waveguide was also optimized for this O-band SOA. Full details are found in [81], [83]. Mainly, the end width of the first stage vertical taper was reduced from 200nm to 100nm to maximize the coupling efficiency. This width reduction results in coupling efficiencies of 98% for TE and 95% for TM. The latter is slightly smaller because the TM field transition point from the active taper to the passive waveguide is closer to the taper tip than for the TE light. In terms of fabrication, this width is possible with better optimization of the process, as discussed in Chapter 5.

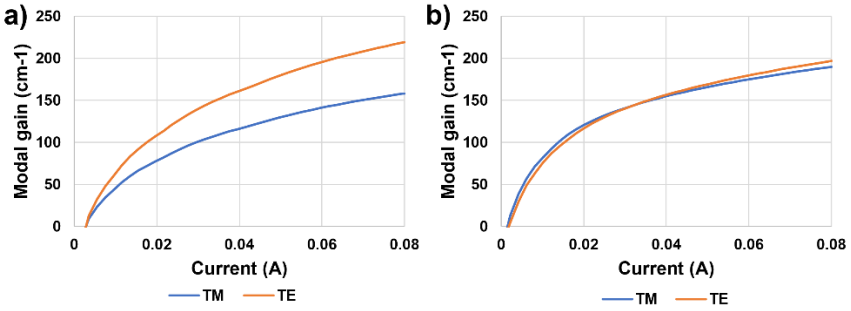

Figure 7.2 C-band PI-SOA modal gain for TE and TM at 1550nm *vs* injection current for 0.5mm-long SOA having an active core with: a) no tensile strain, b) 0,23 % tensile strain

The tensile strain of the active Q was optimized for C-band devices based on a similar approach to the O-band devices. Figure 7.2 show the TE and TM modal gain curves at 1550 nm *vs* injected current for a 0.5mm-long and 2 µm-wide PI-SOA. Figure 7.2.a) corresponds to an active core with no tensile strain, while Figure 7.2.b) shows results for an active core with 0.23% tensile strain. The PDG for the strained stack is below 0.2dB for injection currents in the range of 2-6 kA/cm^2, while it continues to increase at currents higher than 6 kA/cm^2 up to 0.4dB at 8 kA/cm^2. A similar PDG is achieved for wavelengths in the range of 1520-1560nm. The optical confinement values are similar for O-band and C-band. In addition, note that the composition of the active Q core for C-band devices has a lower concentration of phosphorus than for O-band devices. This InGaAs-rich composition has slightly higher free carrier absorption losses, which results from its closer composition to the highly absorbing InGaAs and the smaller bandgap introducing higher free carrier density.

7.2.2 Epitaxial growth and characterization

To realize functional devices with this new epi-stack, several metrology tests were realized to assess its quality before fabrication. The growth was realized in a low-pressure metalorganic vapor phase epitaxy (LP-MOVPE) tool on 3-inch n-type [100] InP wafers. First, the PL peak was calibrated using room-temperature photoluminescence (RTPL), taking into account the blue shift effect that is discussed next. Note that the SOA

is intended to operate at 4 kA/cm². The designed wavelength of 1310nm can be attained by accounting for the 40nm blue shift that takes effect as a result of the band filling effect from current injection. This assumes low heating effects at these current injection levels, since heating red-shifts the peak wavelength as discussed in Chapter 6. So the target photoluminescence (PL) peak is 1350nm. After calibration, the PL peak from the center of the fabricated wafer is shown in Figure 7.3.a). Note that all PL measurements were done before depositing layers 1-6 to avoid absorbing all the light by the InGaAs layers. The PL peak is at 1347.5nm with a STDev of 0.7% across the 2.75-inch area, while the peak shifts significantly for the last 0.25-inch edge. The full width at half-maximum is 97nm, which is close to PL peaks of MQW-based stacks. It is worth noting that for achieving 0.18% tensile strain and emission at 1350nm, the growth requires calibrating the atomic composition within 1% of tolerances. For instance, increasing the Ga composition by 1% shifts the wavelength peak by 20nm. Accurate calibration of strain and composition to this degree is possible, granted by the significant advancement in III-V epitaxy in the last decade.

The C-band PI-SOA is also intended to operate at 4 kA/cm². The designed wavelength of 1550nm is achievable by accounting for a 50nm blue shift effect as a result of band-filling. Hence, after calibrating the reactor based on this, the PL peak from the center of the fabricated C-band PI-SOA wafer is shown in Figure 7.3.b). This peak is composed of two peaks. The active core peak from layer 8 is near 1575nm. The second peak is from the lattice-matched InGaAs etch stop layer (layer 13) at 1650nm. Thus, the full width at half-maximum value of 196.4nm in not precise for the peak from the active region. The PL intensity is slightly lower as well, but this is most likely not related to defects, as the presence of defects lead to a significant decrease in the PL peak intensity.

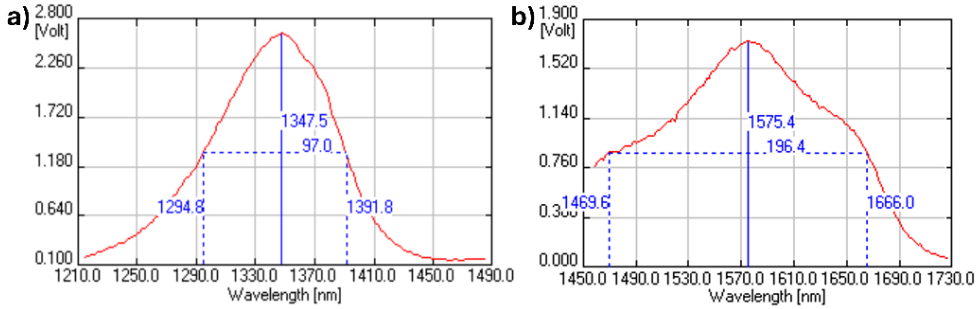

Figure 7.3 PL emission spectrum of the active core used in fabrication of: a) O-band PI-SOAs, b) C-band PI-SOAs

Another crucial aspect for mode propagation and amplification in the SOA is the structural quality and compositional uniformity of layers in the epi-stack. This takes into account the crystal quality of each layer, mainly focusing on those that interact with light, as well as the uniformity of chemical elements in these layers. The crystallographic and compositional properties of the O-band epi-stack were comprehensively analyzed using high-resolution scanning transmission electron microscopy (HR-STEM), and X-ray diffraction (XRD) measurements. Figure 7.4.a) shows HR-STEM images of the stack obtained along the <011> zone axis. The inset focuses on the active waveguiding layers. One main reason for potential defects in this stack relative to previous IMOS stacks is the additional tensile strain in the active

region. Lattice-matched epi-layers have a threshold value in terms of stain and thickness of the strained layer [219]. Going beyond these values relaxes the strain by forming threading dislocations, and these act as recombination centers that provide current leakage paths and increase optical losses via scattering. For this stack, a strain value of 0.18% and thickness of 50nm results in a strain-thickness product of 9%.nm, which is below the critical value measured for InGaAsP-based materials [219]. To verify this, the HR-TEM image of the active core shows no threading dislocations and lattice-matched interfaces between the active Q and SCH layers (Figure 7.4.a). Moreover, the material is uniform in terms of elemental composition, as confirmed by energy dispersive spectroscopy maps taken during TEM imaging.

Note that the strain in fabricated IMOS devices can slightly vary from the original epi-stack layer strain. These slight variations are neglected but are worth to mention. First, the strain of a 2µm wide SOA is not fully uniform across the SOA width, because the structure is slightly relaxed near the mesa sidewalls [220]. However, strain reduction at edge from the 0.18%-0.23% values would be very low, and the mode overlap near sidewalls is also minimal. Secondly, as discussed in Chapter 4, bonding with BCB results in a membrane expansion of 300ppm, corresponding to an additional tensile strain of 0.03%. The effect of the latter on PDG for this stack is minimal, and hence it was ignored as it is close to the fabrication errors. However, the effect was simulated for C-band PI-SOAs by introducing a 0.03% larger strain and assessing the PDG. As a result of increasing the strain from 0.23% by 0.03%, the PDG at injection currents between 2-6 kA/cm^2 increases from 0.2 dB to 0.4 dB.

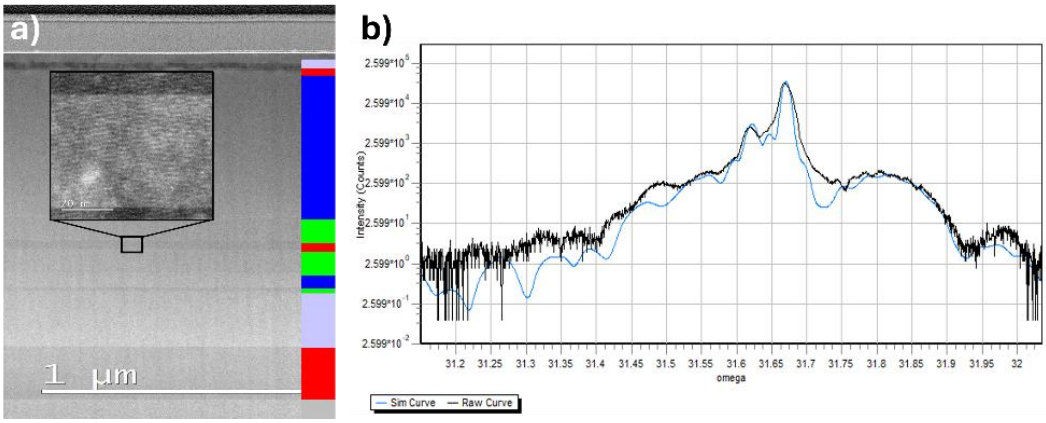

Figure 7.4 HR-TEM image of the O-band stack and corresponding design. Inset: atomic-resolution TEM image of the active Quaternary. b) XRD θ-2θ spectrum of the grown stack, the simulated curve focuses on obtaining an accurate value of strain

Note that the n-type doping level of layers 10 and 11 was slightly lowered to 1.10^{18} cm^{-3} and 2.10^{18} cm^{-3} instead of values shown in Table 7.1. This is to lower the possibility of creating threading dislocations early in the growth, which can propagate upwards to active layers. Finally, Figure 7.4.b) shows the XRD (θ-2θ) spectrum after active layer growth. The curve was simulated for the active part to indicate the tensile strain and composition, which mainly influences the peak at 31.8°. With this, the correct 0.18% strain and composition of the active InGaAsP are verified.

For the C-band stack, the strain value of 0.23% and thickness of 50nm result in a strain-thickness product of 11.5%, which is also lower than the critical thickness for defects formation. Based on this, and the presented PL emission from the C-band stack, further metrology studies using TEM were not carried out for the C-band stack and fabrication continued directly.

7.2.3 Fabrication outcome

Devices were then fabricated according to the SOA/DFB fabrication scheme discussed in Chapter 5, and results are shown next. Figure 7.5.a) shows an image of the fabricated wafer with measured devices zoomed in, while Figure 7.5.b) shows a top SEM image of an SOA, featuring the optical and electrical components of the device. I/O GCs for both TE and TM are connected to the SOA through a PI MMI. It is worth noting that for this run, the average BCB thickness is 1.8µm, and the plated Au thickness is around 4-4.5µm. The latter decreases the resistance of the devices by 2-3 Ω comparing to devices with no plated Au with resistance of 10 Ω. Also, the measured structures have a thermal shunt on the p-side only, which is slightly worse in terms of thermal shunting compared to structures having shunts on the two sides. In addition, the thickness non-uniformity of the waveguiding layer mentioned in Table 7.1 resulted in slightly shifting the optimal wavelength range of the GCs, as discussed in Section 7.6.

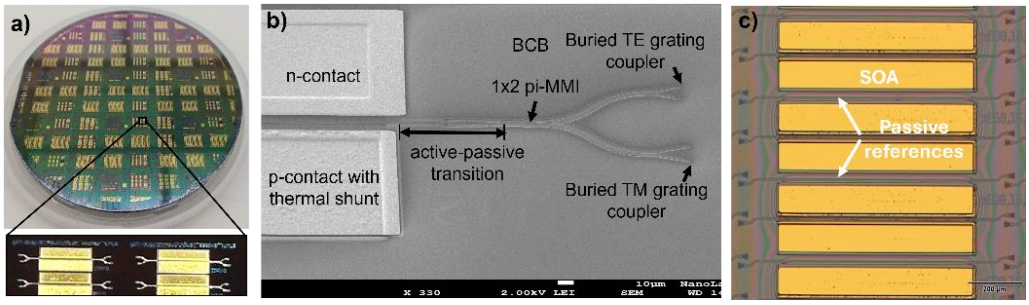

Figure 7.5 a) Image of the fabricated O-band wafer. Inset: measured devices, b) Top-view SEM image of an O-band SOA, c) optical microscope image of C-band PI-SOAs

For C-band SOAs, the design incorporates an array of SOAs paired with GCs of varying pitches to accommodate both TE and TM polarizations, as shown in Figure 7.5.c). The reason for this design is because the gain spectrum of the SOA is significantly broader than the bandwidth of the I/O GCs. By measuring through multiple GCs with closely spaced pitches, it becomes possible to effectively span the full SOA gain spectrum, thereby overcoming the bandwidth limitation imposed by individual GCs.

7.3 Experimental setup

Key characteristics of the SOA, such as transparency curves, net gain for TE and TM light, and PDG were measured using the experiment setup shown in Figure 7.6.a). For this, the full wafer with the DUT was mounted on a copper chuck that was set at 10°C using the cooling scheme discussed in Chapter 6. The gain was measured by the transmission method in DC. Here, light from a tunable laser source is introduced in the amplifier through a polarization converter, while a PD or OSA are used for optical detection.

However, to measure the transparency of the SOA, its junction is interfaced with a Bias-Tee that is linked to a lock-in amplifier (LIA, Stanford SR865A) and a current source (Thorlabs pro8000). The light is modulated at 350 kHz using an arbitrary waveform generator and fed to the laser. The LIA is interfaced with the SOA junction to accurately assess its response to the modulated optical signal for various DC currents via locked-in detection. The electrical signal from the SOA correlates to the SOA's light absorption or gain when the applied bias is below or above transparency, respectively [221], [222]. Hence, for the electrical signal recorded via the LIA, the transparency current corresponds to minima in the signal for each wavelength. Figure 7.6.b) shows a microscope image of an SOA being measured. Here, the SOA is electrically probed and fibers from both ends are aligned to a TE or TM GC, as shown in the GDS. Note that these testing conditions are identical for O-band and C-band PI-SOAs.

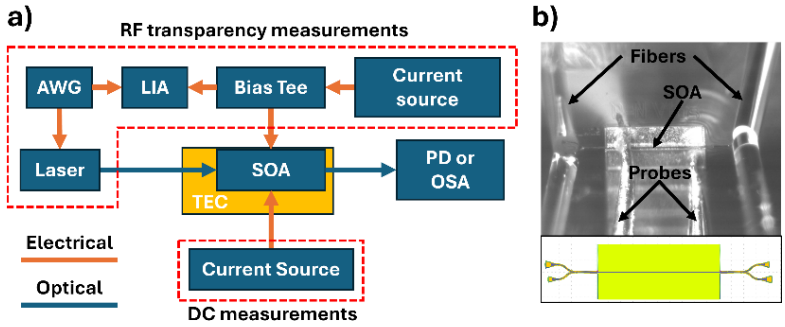

Figure 7.6 a) Experimental setup use to measure SOA characteristics. b) Microscope image of an SOA being measured and corresponding GDS

7.4 Gain and PDG of O-band PI-SOAs

To accurately measure the net gain, the transparency current was first identified. Figure 7.7 shows the transparency current for a 0.5mm-long SOA for TE and TM modes *vs* wavelength between 1280nm and 1360nm. For both TE and TM, the transparency current is below 1.1 kA/cm^2 (11 mA for this SOA length) beyond 1330nm. For wavelengths below 1330nm, the transparency current for TM is more stable than TE because of bandgap shrinkage as a result of tensile strain.

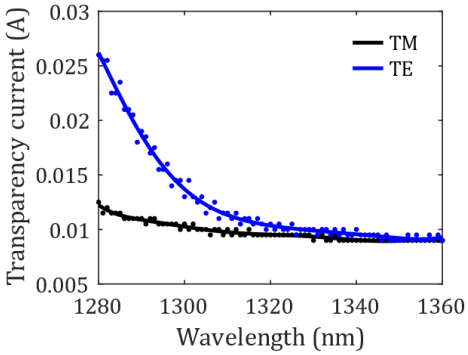

Figure 7.7 Measured (dots) and fitted (lines) transparency current *vs* wavelength in the range of 1280-1360 nm for the 0.5 mm long PI-SOA.

Next, to measure the net gain, optical power is introduced in the SOA for different currents and the output is recorded. The net gain can be calculated by assessing the difference in output power for various currents above transparency and the power at transparency. Via this method, the net internal SOA gain excluding I/O coupling and active-passive losses is accurately measured. Figure 7.8.a) and b) show the net gain at different currents above transparency *vs* wavelengths between 1300nm and 1360nm for TE and TM modes, respectively. The SOA length is 0.5mm and width is 2µm, so these currents correspond to injection current densities in the range of 0.5 kA/cm^2 to 4 kA/cm^2. The peak gain for TE is at 1345 nm with 11.5 dB net gain, and for TM it is at 1340nm with net gain of 8 dB. The blue shift of the peak at this range is 5nm for TE and 10nm for TM, which are below the expected 40nm from design. The 40 nm shift would result from the band filling effect excluding any thermal effects. However, as shown in Chapter 6, even for thermally shunted SOA-based devices, thermal effects still exist and is especially prevalent for InGaAsP-based devices compared to Al-based devices [223]. Having a thermal shunt only on one side for these devices also reduces their effectiveness. The self-heating red shifts the gain peak, which counters the band filling effect and results in lower overall wavelength shift *vs* injected current. Moreover, the gain saturates for currents beyond 25mA, and possible reasons for this will be further discussed below.

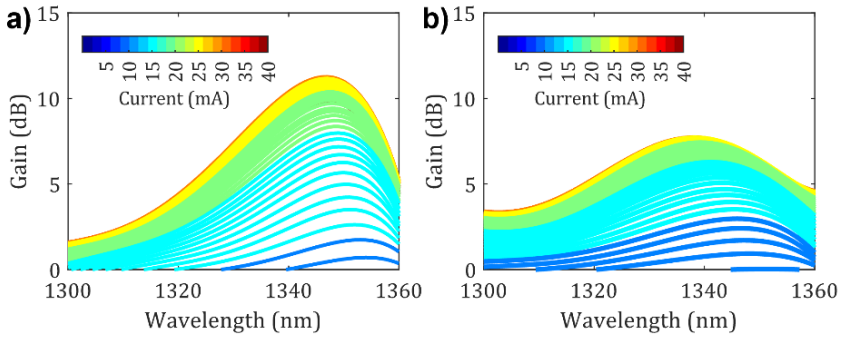

Figure 7.8 a) 0.5mm-long and 2µm-wide SOA gain *vs* wavelength for currents between 5mA and 40 mA for: a) TE b) TM

Figure 7.9.a) shows the PDG *vs* wavelength at current of 25mA, as calculated using Eq.(17). The minimum PDG range is for wavelengths between 1312nm and 1337 nm, with PDG below 1dB. This corresponds to a net gain at 1337 nm of 8.5 dB for TE and 7.5 dB for TM. Here, the SOA can be considered as polarization insensitive for this wavelength range and current. Moreover, the PDG is below 2.5dB for wavelength between 1300nm to 1343nm, and 1353nm to 1360nm, covering most of the gain bandwidth of the SOA. Figure 7.9.b) plots the PDG *vs* current up to 40mA and for wavelength of 1320nm. Here, the PDG is well within 1 dB for currents below 30mA. Beyond that, the gain saturates and PDG increases because of further redshift of the TM gain, as shown in Figure 7.8.b).

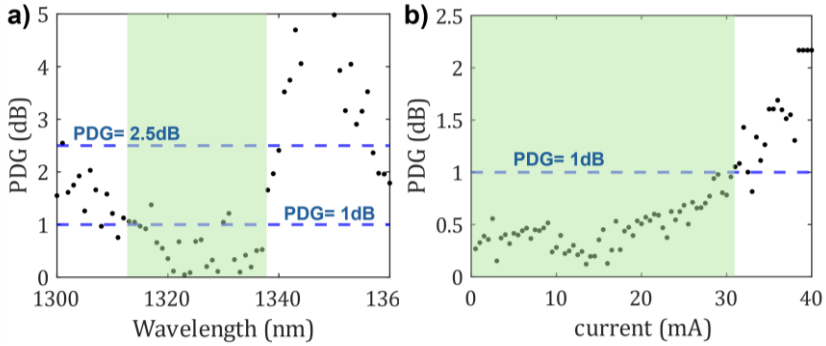

Figure 7.9 0.5mm-long and 2µm-wide SOA: a) PDG *vs* wavelength at current of 25mA, b) PDG *vs* current at wavelength of 1320nm.

Results shown above were measured after removing the BCB planarization layer. After fabrication, the GCs functioned at an optimal wavelength beyond 1360nm, which is higher than the SOA gain peak. So one possible way to fix it was to remove BCB, which increases the effective index of the grating and lowers the transmission wavelength. BCB removal shifted the wavelength towards lower values, slightly reducing the insertion loss, but it also degraded the optical response of the SOA. The mechanism behind this is explained next. Preliminary measurements were realized before BCB removal to avoid introducing more particles in the wafer. Figure 7.10.a) shows the output power at the transparency and at injection current of 40mA before the BCB removal. The resulting net gain for TE is shown in Figure 7.10.b). It can be seen that a net gain of up to 19 dB at 4kA/cm^2 is achieved. The net gain increases for currents up to 4kA/cm^2, while after the BCB removal, it only increases for currents up to 2.5kA/cm^2. There are two possible reasons for this degradation. First, RIE etching of BCB in CHF_3 plasma also effects the Au metallization. But the diode resistance before and after etching is similar, therefore this is less likely. Secondly, because the process was realized on the full wafer with no lithography mask, BCB was removed from the SOA sidewalls as well. This could affect the quality of surface passivation and shift the mode slightly to one edge of the SOA, and hence lead to lower injection efficiency and higher internal propagation losses.

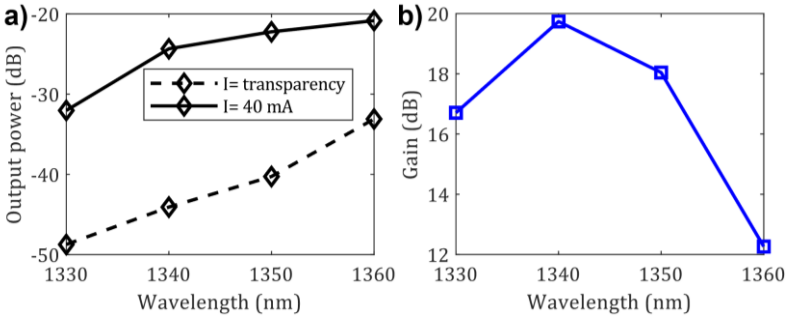

Figure 7.10 Measurements before BCB cladding removal of a 0.5mm-long and 2µm-wide SOA: a) output power at transparency current and 40mA current, b) net gain at 40mA.

Measurements of the output saturation power was not possible because of the high losses of the GCs and limited laser power that can be supplied. These GCs have low 3dB

bandwidth that needs to be well aligned with the SOA gain peak. Moreover, the gain peak is broader, as can be seen in Figure 7.8. For such devices, an ideal way for fiber-to-chip coupling is to use broadband SSCs via edge coupling.

Finally, further developments can focus on improving the gain medium heat sensitivity by using the methods discussed in Chapter 6. The design of the device should take into account this sensitivity, as well as other factors that could affect the material parameters to achieve a gain peak at 1310nm with minimal PDG. Also, the active-passive transition based on this bulk active was not measured because the test devices were not included. This is an important factor to quantify and decide on further development for the active-passive integration interface. Additionally, the epi-stack thickness variation needs to be controlled within tolerance below 5% to guarantee high yield and uniformity of device performance across the wafer area.

7.5 Preliminary measurements for C-band PI-SOAs

For C-band PI-SOAs, only preliminary measurements were realized to plan for a more comprehensive study at a later stage. A 0.75 mm-long SOA was measured using the transmission method in TE mode to assess the net gain. Figure 7.11.a) shows the TE ASE spectra *vs* wavelength from this SOA. The top red curve corresponds to the transmission through a passive reference structure, which is composed of a GC-waveguide-GC where the passive waveguide has the same SOA length. Here, the transmission through the passive reference is more intense than the ASE spectrum from the SOA. This is likely caused by high losses in the active-passive transition, as will be further detailed below. Figure 7.11.b) shows the output power at the transparency current and at 35 mA injection current. The net gain here is approximately 1.5–3 dB for wavelengths in the range of 1530–1630 nm. Additionally, the saturation power was measured for a 1550 nm wavelength at currents ranging from 20–40 mA. The optical I/O power relationship remains linear at input powers of up to 5 dBm. However, this input power level is already considerable for saturation, which confirms the high loss from the active-passive transition, as seen in Figure 7.11.

The high losses and low gain observed in this SOA can be attributed to several factors. First, the active-passive transition introduces significant optical losses compared to the O-band transition. This is because the first stage of the twin taper includes the active core layers and has a length of 30 μm, but it is not electrically pumped. Consequently, taper losses here are likely higher because of the InGaAs-rich core composition that increases absorption. Moreover, the lower net gain and ASE intensity for the C-band stack compared to the O-band stack might result from the higher free carrier absorption losses. Simulations for both of these epi-stacks were realized in an isothermal environment, whereas IMOS devices are more prone to self-heating. This can affect C-band devices more significantly as a result of their smaller bandgap, which enhances the Auger recombination rate compared to O-band devices, consequently increasing heat generation [224], [225]. Finally, the tensile strain is below the critical thickness. However, the epi-stack was not analyzed via TEM imaging to confirm if the active core is completely free of defects. If present, these act as non-radiative recombination centers and contribute to localized heating, thereby further increasing losses and reducing the device efficiency.

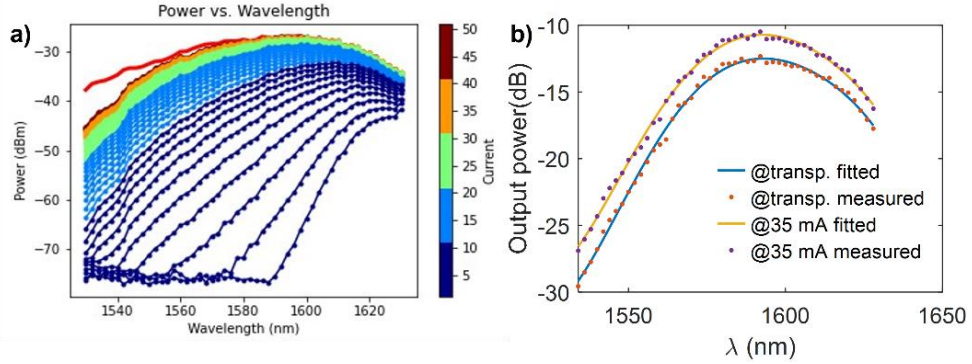

Figure 7.11 TE transmission measurements *vs* wavelength from a 0.75mm-long C-band PI-SOA, a) ASE spectra *vs* injected current, b) output power at transparency current and 35mA current

A comprehensive measurement plan is necessary to have a full understanding of the SOA performance. However, to address the potential issues identified, several strategies can be implemented. First, a butt-joint type of active-passive transition is preferable for both of these bulk stacks. The butt-joint transition does not contain the taper with the unpumped active core. Therefore, with proper design considerations to minimize mode mismatch and scattering losses, it could be a more effective option. Secondly, regarding the active core composition, employing strained MQWs for PI performance could enhance carrier confinement and reduce the free carrier density, making it a better option for C-band PI-SOAs on IMOS. Additionally, both the C-band and O-band PI-SOAs presented here could benefit from the full thermal strategy outlined in Chapter 6 including shunting on both sides, as well as the improvements on thermal shunting discussed in Annex B.

Figure 7.12 shows the TE optical signal-to-noise ratio (OSNR) versus wavelength for the 0.75 mm-long C-band PI-SOA at 35 mA injection current. The OSNR increases from 25 dB at 1530 nm to 40 dB at 1575 nm, then stabilizes for wavelengths between 1575 nm and 1630 nm at values slightly above 40 dB. The OSNR values are promising for measurements on broadband amplification and high bit rate data transmission over the C-band and L-band (1565 nm to 1625 nm).

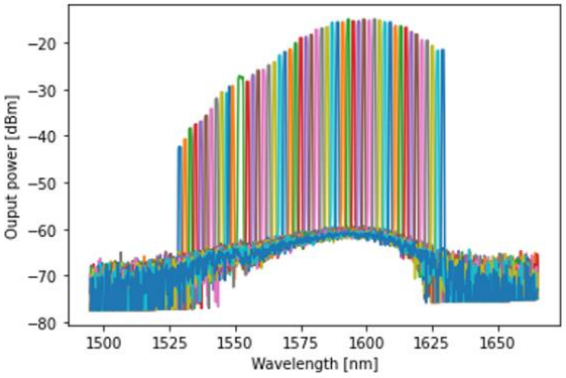

Figure 7.12 TE OSNR *vs* wavelength for the 0.75mm-long C-band PI-SOA at 35mA

7.6 Fabrication tolerances of C-band and O-band GCs

Following the standard I/O fiber coupling method to IMOS PICs, focusing GCs [12] were used in this thesis for all fabrication runs[106]. The epitaxy for C-band and O-band PI-SOAs was realized in-house with a reactor originally built for 2-inch substrates, while the used wafers are all 3-inch in size. This results in non-uniformities in layer thicknesses up to 10-12% as shown in Table 7.1. The effect of this non-uniformity could be especially important for the GC performance, where tolerances for thickness non-uniformities needs to be checked for both C-band and O-band GCs.

For instance, all C-band GCs function close to the targeted optimal wavelength. However, the first generation of O-band devices in IMOS were realized within the O-band PI-SOA run discussed here. These functioned at a wavelength of 1410nm in the center of the wafer and 1360nm at the edge of the wafer, so only devices in the edge were measurable. Note that the thickness of the waveguiding layer in that run vary between 315nm to 285nm from center to edge. Hence, this discrepancy prompted the following study on GC tolerances to thickness variations in the waveguiding layer. The gratings pitch Λ is calculated using the following equations [226].

$$\Lambda = \frac{\lambda}{n_{eff} - \sin(\theta)} \tag{18}$$

$$n_{eff} = F.\, n_s + (1 - F) n_e \tag{19}$$

where λ is the central wavelength, θ is the angle of incidence, n_{eff} is the effective index of the grating, considering an etch depth of 120nm. The latter is calculated using Eq.(19), where the filling factor F is 0.5, and n_s and n_e are the effective indices of the slab waveguide thickness and the etched thickness for the grating, respectively. The latter can be calculated using Lumerical Finite Difference Eigenmode solver. Calculation of the optimal pitch for C-band and O-band GCs was realized for waveguiding layer thicknesses in the range of 270-330nm. The optimal pitch for a waveguide thickness of 300nm matching the design thickness is 522 nm and 653 nm for TE and TM in the O-band, and 655 nm and 862 nm for TE and TM in the C-band, respectively. To compare the tolerance in fabrication of O-band and C-band GCs, the pitch was normalized to the pitch in the ideal waveguide thickness of 300nm. The chosen etch depth for the gratings is 120nm and this is achievable with wafer-scale non-uniformity below 5nm using dry etching, thus this is kept fixed. Results are shown in Figure 7.13. Deviations in the waveguide thickness in the range of 270-330nm lead to similar pitch tolerances for the O-band and C-band, with maximum variations around 4% for TE and 7% for TM respectively. For the previously discussed O-band devices in this chapter, the pitch was 548nm for TE and 749nm for TM, which are not optimal for O-band operation and resulted in high losses. This was fixed for the UTC-PD run that came after, where O-band PDs work as intended.

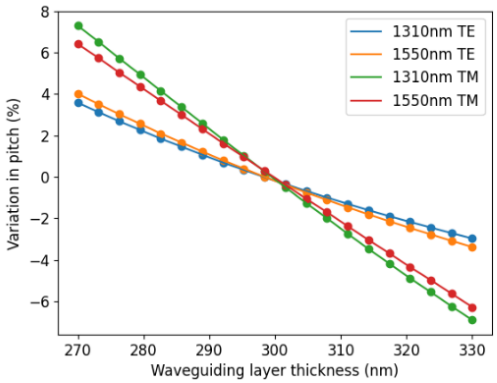

Figure 7.13 Variation in the optimal pitch for O-band and C-band GCs *vs* waveguiding layer thickness

7.7 Conclusion

In this chapter, O-band PI-SOAs based on tensile-strained InGaAsP bulk active core were introduced to the IMOS platform. From simulations, a 0.5mm-long SOA exhibits net gain beyond 15dB at 4kA/cm^2, and PDG lower than 1dB for a large bandwidth of 1270-1340nm. Experiments show that SOA exhibits high net gain with value of 11.5dB at 1350nm for low current injection of 2.5kA/cm^2. The PDG is also below 1dB for a bandwidth of 25nm. Moreover, the SOA gain before removing the claddings reached up to 19 dB as a result of better surface passivation. This energy efficiency provided via a thin gain medium makes these PI-SOAs suitable for high density integration needed in large-scale applications and for applications requiring efficient standalone SOAs. For C-band PI-SOAs, the design is capable of maintaining PDG below 1dB across a 40nm bandwidth and current densities in the 2-6 kA/cm^2 range. Finally, the fabrication tolerances of C-band and O-band I/O GCs is shown to be similar for both TE and TM, noting that TM requires lower tolerances than TE for the two bands.

Chapter 8
Towards a first InP 3D E-PIC receiver module

This chapter explores the co-design and fabrication of a co-integrated receiver module that combines an IMOS receiver circuit with III-V lab drivers, validating the co-integration methodology discussed in Chapter 2. A key feature of this approach is the compact design of the 3D E-PIC module, short interconnects, and low power devices, which minimizes size, cost, and power consumption. The discussion begins with an evaluation on the availability of electronic and photonic devices, focusing on their compatibility and performance within the receiver architecture. This is followed by an in-depth look at circuit design layout and wafer assembly strategies. Finally, a scalable approach to 3D E-PIC design is proposed. It emphasizes on using unified compact models and leveraging a unified PDK that integrates electronic and photonic devices along with comprehensive DRCs. This unified approach ensures design robustness and scalability, facilitating the implementation of these modules for future technologies. [6]

8.1 Circuits design

The full transceiver architecture featuring interconnected EICs and PICs was previously shown in Chapter 2. For the first co-integration demonstrator, the receiver side was chosen to reduce complexity and manufacturing risks. This is because all crucial photonic components for the receiver have been demonstrated and are more mature than the required photonic transmitter components. A schematic architecture of the receiver's PIC is shown in Figure 8.1. The optical input consists of a two GCs for TE and TM polarizations, connected with a 1×2 PI-MMI, which could be replaced with a single

[6] For contributions, partners from III-V lab (headed by Romain Hersent) guided the circuit design of the co-integrated driver, Virginie Nodjiadjim helped in providing the EIC layout and discussions.

PI-SSC in future work. This is followed by a pre-amplifying SOA to amplify the signals before demultiplexing using a PI-AWG. The latter routes signals from each wavelength to a UTC-PD that is connected to the TIA-ADeMUX EIC.

Figure 8.1: Simplified architecture of the optical part of the receiver

In terms of the availability of photonic BBs, TE and TM passive BBs, PI-MMIs, AWG, PI-SOAs, and UTC-PDs are available. The PDs are inherently PI, because the InGaAs absorption layer is polarization agnostic. The UTC-PDs also function for C-band and O-band thanks to the InGaAs absorption layer. However, several PIC device and platform developments are required to achieve this architecture. First, the AWG requires a new design for polarization insensitivity. This needs to account for several fabrication factors to achieve low insetion loss and high crosstalk ratio between channels [75]. Secondly, the SOA and UTC-PD need to be integrated within the same platform, requiring a new epi-stack and fabrication steps. This is an ongoing research [72], [74], [105]. Thus, in terms of photonic devices, this was reduced to a single channel where the PI-AWG and SOA are omitted, and only TE polarization is used for the demo circuit.

In terms of EICs development, the TWILIGHT project realized dedicated runs for transmitter InP DHBT linear drivers. On the other hand, receiver TIAs were developed within MPW runs, so these are only available as individual chips. However, UTC-PDs can still be integrated with the DHBT linear drivers. The generated photocurrent from the improved PDs is adequate to be converted to a voltage swing of the voltage-mode driver, as detailed next. This compromise ensures the possibility to demonstrate a fully functional InP-based E-PIC at lower manufacturability risks.

The first generation of 3D devices was planned based on the previously developed process flow in Chapter 2. The co-design plan was realized as a joint effort between III-V Lab and TU/e, benefiting from the available devices discussed earlier. Figure 8.2 shows the E-PIC circuit architecture. It features the PD-amplifier TPV interconnections in black, input DC pad from photonics as green, and output DC and RF pads from electronics as red. The driver has a total of 5 pads for DC bias and controls and 4 RF pads (2 inputs and 2 outputs terminals). The RF pads are implemented in a GSGSG configuration. A single PD is connected to one of the driver inputs, and around 1-2mA of photocurrent is required to achieve the required voltage swing of the driver. This is possible by using the PDs developed in Chapter 6. A 50-Ohm termination (see chapter 5) is placed between the driver input and the ground in order to convert the current from the photodiode to feed the voltage-mode driver IC. The linear driver is implemented in a differential configuration, so its input signals should have a 180° phase-shift with respect to one another. Since a phase shifter is not yet compatible with the UTC-PD stack, the unused driver input is connected to a 50 Ohm termination for more symmetry.

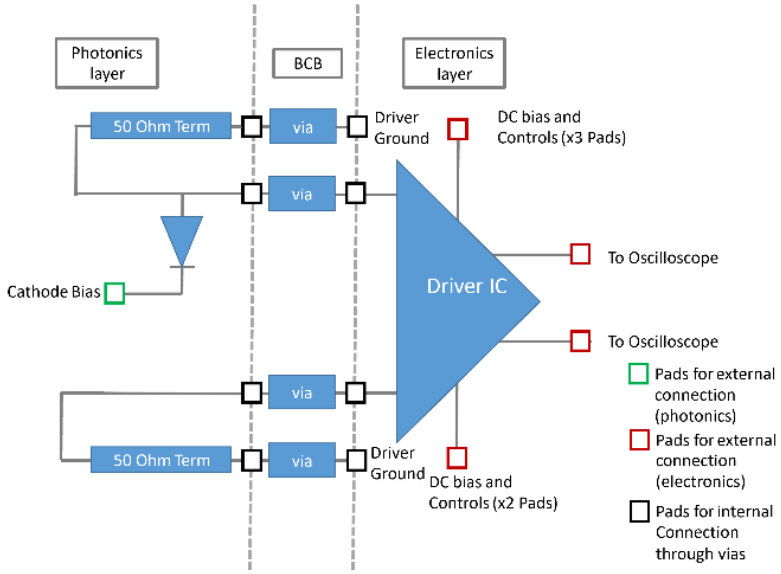

Figure 8.2 PD-amplifier E-PIC circuit architecture

Note that 3D integration of InP UTC-PDs with InP DHBTs is not only interesting in data communication, but also to advance millimeter-wave technologies for use in other applications, such as 6G wireless communication. Monolithic integration of these devices via epitaxial regrowth on a single wafer is already being investigated [27]. As discussed earlier in Chapter 1, this approach poses high technical and design challenges, so 3D integration could be an option to reduce these risks while offering shorter interconnect distances.

8.2 Layout and co-design considerations

8.2.1 Co-design of the optical and electrical components of the E-PIC

III-V lab fabricated EIC drivers on a dedicated wafer whereby the dimension of each reticle is 1.2×1.5 mm^2. 12 different designs are compiled in an array of 3×4 reticles, yielding a super reticle of 4.8×4.5 mm^2 that repeats throughout the wafer. The co-design layout of the photonics, and its reticle size and placement considerations, were matched to the electronics layout and reticles distribution. The goal of co-design is to achieve the shortest RF distance between the active UTC-PDs and the driver inputs to minimize signal losses. This is possible by placing the UTC-PDs close to the driver input. Figure 8.3 shows the GDS layout of the photonics layer, featuring photonic devices in purple, openings of the EIC driver pads in blue, the TPV BCB open in striped green, and the plated Au in yellow. The light orange rectangles around the edge correspond to BCB anchors, which have an identical fill factor of 20% as in Chapter 3. The distance that RF signals have to travel between the PD and the driver input is 300µm. This value was set according the following considerations, but further scalability is discussed in Section 8.4. First, a 75µm-long resistor is inserted between the CPW lines. This length, together with a separation of 10µm between the metals contacting the semiconductor (matching the CPWs GS separation), corresponds to a resistance of 50 ohm. Note that a NiCr

resistor is more favorable [60]. However using a vertical resistor fabricated from the EIC side is not possible as the electronic substrate targeted transmitter components and were already fabricated. Secondly, this takes into account a possible misalignment of 10µm in any direction, which represents the worst-case-scenario when anchors are used. As a result, the PD is placed farther away from the driver's RF input to allow for post-bonding misalignment compensation for the TPVs lithography masks if the photonics layer is shifted in the horizontal direction.

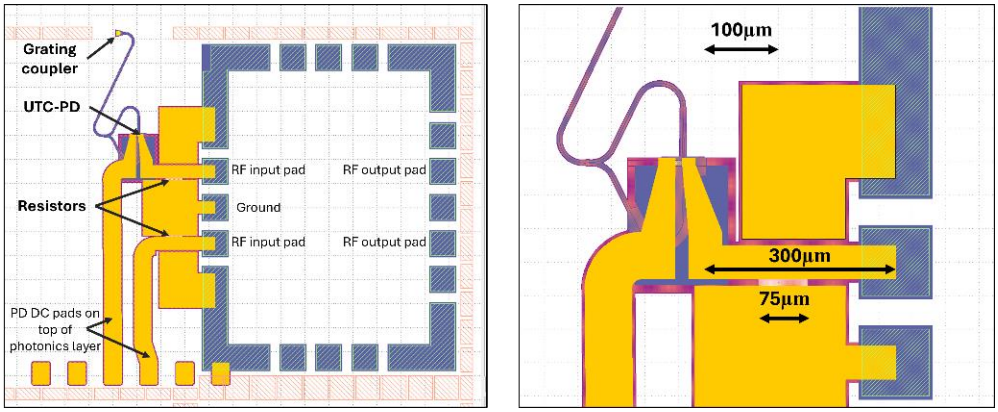

Figure 8.3 GDS layout describing device placement and a zoom into the PD region

As discussed earlier, the photonic semiconductor layers are removed everywhere around Au plating regions and EIC pads. These layers can significantly increase the RF losses of CPWs on top of the membrane. After removing these layers and planarizing the photonics with BCB, the CPWs lie on top of a BCB layer with total expected thickness of 11µm, *i.e.*, 10 µm for bonding and 1 µm for planarization. This high BCB thickness provides an effective shield for the CPW lines from the substrate below and structures present there. This is because the design shown in Figure 8.3 is on top of a neighboring reticle that contains EIC components, as discussed earlier. As a result of this BCB thickness, low CPW and TPV losses are expected [46]. Based on measurements presented in Chapter 2, the total losses from the 300µm CPW and TPV are expected to be around 1 to 1.5dB in the case of having rough BCB on the top.

As for optical routing, all optical functionalities are realized within the photonic layer with high design freedom on the membrane. The UTC-PD is placed close to the driver input. However, the GC relies on the back reflections of light coming from the substrate. So the GC was placed in a region where the InP substrate has no patterns or other materials such as metals or epilayers except for the SiO_2 and BCB used for bonding. This corresponds to the diceline region at the edge of the EIC reticle. Despite the lack of back reflectors, this is expected to mitigate the risk of low optical coupling to the E-PIC. It comes at a cost of slightly longer passive waveguide connecting them to the PD, but the length is less than 0.25mm, which contributes to less than 2dB loss considering the quality of usual EBL-made waveguides.

In terms of thermal performance, the electronics and photonics in this layout share the same substrate and are integrated close to each other. Hence thermal degradation from crosstalk between devices needs to be considered. In Chapter 6, it was shown that the thermal footprint of UTC-PDs is highly localized in the diode area. The thermal

hotspot of the driver circuit is also highly localized where most DHBTs are concentrated. The EIC and PIC hotspots are placed far apart and result in low thermal crosstalk.

The topography of the 3D E-PIC and its plan for optical and electrical probing are shown in Figure 8.4. The height of the different components has been taken into account to allow for probing all devices on-wafer after front-end fabrication. Both RF and DC connections as well as the input optical fiber positions were carefully considered for rapid and reliable experimental characterization without the need of dicing. This is possible by providing the optical input at the PIC interface from the west side of the E-PIC, and the RF probes at the driver output ports from the east side of the EIC interface. DC biasing of the PIC and EIC ports is achieved both from the north and south of the E-PIC via probe array cards. Note that EIC components can be reliably analyzed on-wafer using VNAs [227].

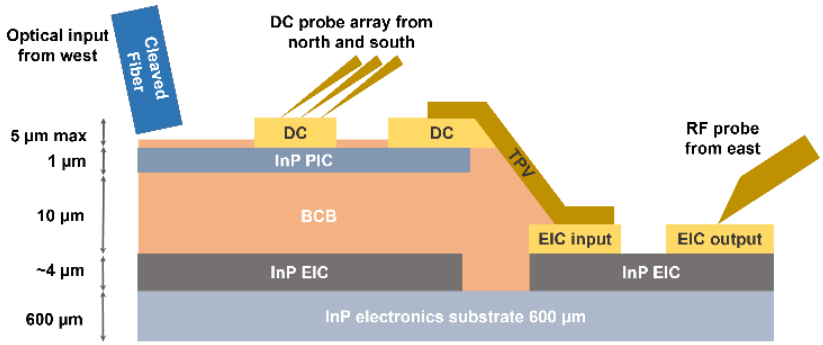

Figure 8.4: Schematic cross-section of the 3D E-PIC and its probing plan

8.2.2 Wafer assembly from the photonics side

Similar to the discussion in the previous section, wafer assembly was also realized based on the super reticles in the available EIC substrate. The PIC reticle dimensions match that of the EIC super reticle, as highlighted by the dashed line in Figure 8.5.a). To maximize the yield when populating the wafer layout, the majority of the electronic drivers have been characterized at III-V lab before shipping to TU/e for co-integration processing. Note that two drivers are available for each EIC super reticle, so this characterization revealed the status of these drivers. The PIC devices layout on each super reticle was then chosen based on the outcome of this pre-shipping characterization. To maximize the number of co-integrated receivers with functional photonics, six types of PIC super reticles were realized and assembled on the photonic wafer matching the EIC substrate, as shown in Figure 8.5.b). The green reticles have both drivers working, the orange and yellow reticles have one of the drivers working (top or bottom in Figure 8.5.a), while the drivers in the red reticles are not functional. The free areas in the mentioned reticles is used for reference photonic devices or circuits. These include standalone UTC-PDs, passive BBs, resistors, and RF de-embedding structures. For the blue areas, all contacts for the 12 EIC reticles are opened for direct measurements. These serve as a reference to monitor and assess any unforeseen impact from bonding and 3D integration post-bond processes on the driver IC, such as the quality of plating. Other designs within the blue super reticles include single DHBTs, IC circuits, and test structures. Finally, the black areas are reserved for

large EBL marker arrays. This layout arrangement resulted in 20 design variations for the co-integrated E-PICs, and around 5-7 copies per configuration. Variations for each design were carefully chosen to span a sufficient parameter space via principles from the design of experiments. The design variations are distributed according to a spiral configuration from the center to achieve a more uniform distribution of all different designs.

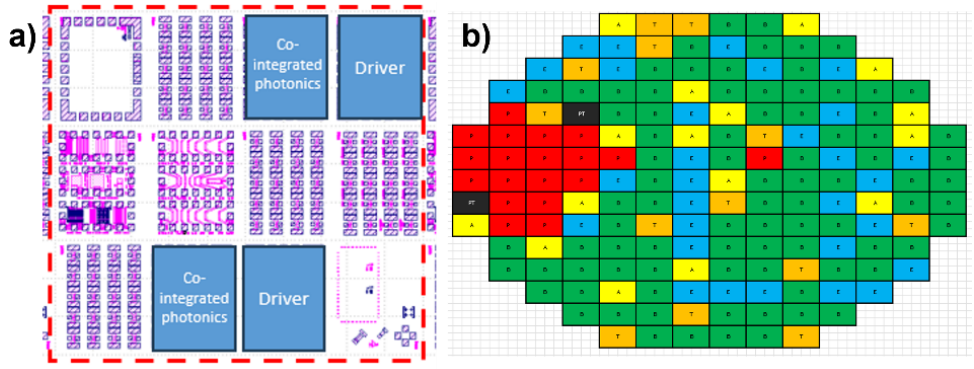

Figure 8.5: a) EIC super reticle design featuring the 2 possible locations for co-integrated E-PICs. b) Wafer assembly mapping of all super reticles, the major flat is on the left side.

8.3 Results and progress

The fabrication plan featured two PIC wafers. The first wafer aimed to validate the fabrication flow of the UTC-PD with plated Au and to serve as a front runner for the actual co-integration wafer. Its results were reported in Chapter 6. The second wafer was dedicated for co-integration. Its pre-bond steps were all successfully implemented in III-V lab and TU/e cleanrooms, for EICs and PICs respectively. Note that the process flow for the PIC wafer was described in Chapter 5. Images of these wafers after all pre-bond processing are shown in Figure 8.6.a) and .b), respectively. For the photonics wafer, the SiO_2 deposited before making anchors also functions as an etch-stop during the BCB anchor etch. Hence, the difference in colour in Figure 8.6.b) comes from a difference in SiO_2 thickness between the center and edge of the substrate. The inset in Figure 8.6.b) is a microscope image of the PICs wafer focusing on the co-integration receiver design and BCB anchors.

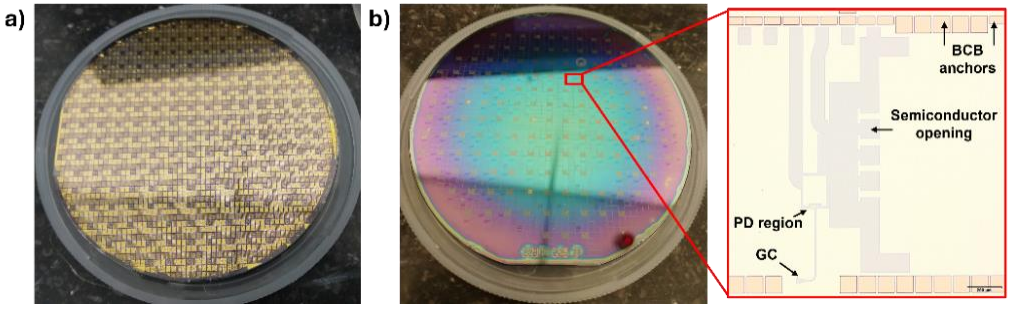

Figure 8.6 Images of the wafers just before bonding: a) EIC. b) PIC. Inset: microscope image of the photonic devices buried under SiO_2 also showing BCB anchors

Adhesive bonding was realized according to the optimal parameters discussed in Chapter 2. Next steps involve depositing the multilayer coating to remove the photonics wafer, then further processing on the photonics membrane. However, ALD deposition of SiO_2 that acts as protective coating was not possible because of a long down time of the tool, which hampered the fabrication progress at the time of writing this thesis. Another solution that is being pursued is using ICP-CVD SiO_2 instead. It involves a higher risk of forming etch pits at the wafer edge, but it will allow for verifying the bond quality as well as continuing post-bond processing.

8.4 Towards a scalable 3D E-PIC design PDK

3D E-PICs are only scalable if they benefit from the full potential of this integration method by realizing ultra-short interconnects and high-density circuitry. The 300um RF separation between the PD and driver input was mainly chosen as a result of the presence of a long membrane resistor in-between, and considering the discussed manufacturing constraints. This separation can be significantly reduced to <15µm. First, this is possible by eliminating the resistor and co-integrating receiver photonics with an EIC TIA instead. Secondly, using state of the art tools such as scanner lithography or laser writing can further improve the manufacturing tolerances, to limit the main separation to the post-bonding misalignment.

For scalability of this co-integration approach, extensive simulations incorporating compact models of the PIC, EIC, and TPV within a unified interface are essential. A key aspect of this is the realization of a combined equivalent circuit model including the PD and TPV alongside the driver, enabling a full co-design strategy to optimize the interfaces for high-speed performance.

Furthermore, The technology also needs to be accessible to external designers at a low knowledge barrier. Thus, building a single joint process design kit (PDK) for 3D integrated E-PIC devices is crucial. Ongoing research is being conducted to identify the key characteristics essential for this [48]. This is because 3D devices need to respond to many challenges on multiple scales. For instance, realizing ultra-short interconnects requires close proximity of photonic and electronic devices. This is only possible if the thermal crosstalk is quantified, and simple design rules or checks are implemented within a common PDK. Similarly, other co-design rules here could be translated as a design rule check (DRC) list within the PDK. The latter ensures that these rules are respected while fabrication details remain confidential with minimal exposure. Asides from the regular DRC checks for PIC devices, such as waveguide and electrical connectivity, new checks could be implemented such as the following:

- Restricted placement of the optical I/O
- Proximity of heat sources at the EIC and PIC interfaces
- Impedance-matching-aware electrical connectivity rules, including width mismatch and discontinuities. The TPV could also be implemented as a black box
- Other rules related to packaging the 3D EPIC, especially if double side active cooling is implemented

A common PDK with these DRC checks can be implemented on software or libraries allowing for both EICs and PICs design. This only needs to take into account supporting

the top-down design approach of complex EICs, which is often realized via dedicated software like Advanced Design System.

8.5 Conclusion

In conclusion, this chapter detailed the co-design and fabrication of a co-integrated 3D E-PIC receiver module, demonstrating the feasibility of integrating IMOS UTC-PDs with III-V lab drivers. A simplified receiver photonic circuit was chosen to mitigate fabrication risks and benefit from mature components. The study explored critical aspects, including device compatibility, circuit co-design methodologies, wafer assembly strategies, and fabrication constraints. A key outcome was achieving a short separation distance between the UTC-PD and the driver input, with potential scalability below 15μm through advanced fabrication techniques and co-integration with TIA EICs. Furthermore, the chapter discusses the need for a unified PDK tailored for 3D E-PICs, ensuring robust DRC definitions that address optical and electrical connectivity, thermal management, impedance matching, and packaging constraints. Overcoming these challenges is crucial for scalable and manufacturable 3D E-PIC solutions.

Chapter 9
Conclusions and perspectives

9.1 Conclusions

This thesis focused on developing and optimizing technologies to enable 3D integration of InP-based E-PICs for high-speed applications. The photonics are based on the IMOS platform, while the electronics are based on the InP DHBT technology. The work addressed critical challenges regarding process compatibility, bonding technology, thermal management, and design of PIC devices. It culminates with a cohesive fabrication run for a scalable and energy-efficient 3D receiver E-PIC.

First, the compatibility of electronics with 3D integration was thoroughly assessed. A process temperature cap of 240°C was established to ensure that the performance of DHBTs remained uncompromised during bonding and post-bonding steps. Protective coatings were developed to enable the wet removal of the photonics substrate without damaging the electronics carrier, ensuring a robust and reliable fabrication process. Co-design rules were established to guide the design of functional E-PICs, accounting for fabrication tolerances, and optical, electrical, and thermal constraints. Experiments demonstrated RF losses as low as 1.2 dB/mm for thick CPW lines on BCB and an additional loss of only 0.4-0.5 dB per TPV interconnect at 67 GHz, demonstrating the potential for high-speed, low-loss interconnects. Thermal management studies revealed hotspot regions of EIC drivers, enabling DFB lasers to be placed with a 100µm offset to high-power EIC regions, preserving the device performance and the high density granted by 3D E-PICs.

The post-bond alignment and bond uniformity were significantly improved by introducing BCB-based anchors into the bonding process. This innovation addressed the alignment degradation caused by reflow in soft-baked BCB. By using BCB anchors, the alignment accuracy improved by an order of magnitude for BCB thicknesses in the 2-16 µm range, approaching the fundamental pre-bond alignment accuracy of the tool. The thickness uniformity improved by a factor of 2-3x for BCB thicknesses in the 8-16 µm range. Bonding with BCB anchors and soft-baked BCB maintains the void-free quality and bond layer uniformity in terms of physical and mechanical properties.

Wafer-scale membrane spatial distortions induced by the bonding process were accurately studied using e-beam metrology. The substrates CTE mismatch results in linear expansion with values reaching up to 300 ppm when bonding InP membranes to other substrates (e.g., Si, SiC). Bonding InP to InP resulted in negligible linear expansion. Residual distortions were quantified and found to be small regardless of BCB bond thickness, opening future avenues for enabling scanner lithography on IMOS devices.

This work also focused on developing thermal management strategies for membrane devices. This is realized by implementing efficient thermal shunts connecting isolated membrane devices to the substrate. These shunts are an inherent part of the cohesive 3D E-PIC fabrication flow as they act as TPVs. First, energy-efficient DFBs using 5µm-thick thermal shunts were developed, resulting in significant performance improvements. This includes I_0 values as low as 0.77 kA/cm^2, SMSR exceeding 50 dB, and thermal resistance values of 176 K/W and 115 K/W for 0.5mm and 0.75mm DFB lengths, respectively.

Secondly, UTC-PDs targeting better power handling were demonstrated. Single injection PDs with 3µm-thick thermal shunts demonstrated 2.34× improved power handling relative to baseline PDs, a maximum DC external responsivity of 0.46 A/W at -4V for a PD of 2.92×3 µm^2 area, and 3dB bandwidth exceeding 67 GHz. Dual-injection PDs with 3µm-thick pads on BCB improved power handling by 3.95× relative to baseline PDs, with 3dB bandwidth exceeding 67 GHz for photocurrents of 4.3 mA. Both of these PD types with dimensions of 10.24×3 µm^2 demonstrated a linear RF output power up to photocurrents close to their maximum power handling capacity. Additionally, the thick metallization used for thermal shunts also contributed to lower RF transmission losses in CPW lines and TPV interconnects, further enhancing the performance of 3D-integrated devices.

Polarization-insensitive O-band SOAs based on a tensile-strained bulk active core and thermal shunting demonstrated high gain above 10 dB and low PDG below 1 dB at small current densities of 2.5 kA/cm^2, making them suitable for high-density and low-power applications. The design of C-band PI-SOAs maintains PDG below 1dB for wavelengths between 1520-1560nm. However, preliminary measurements of a 0.75mm-long C-band PI-SOA reveal limited gain and high active-passive transition losses, which will be further investigated.

Finally, a hybrid E-PIC module was co-designed by integrating UTC-PDs with DHBT drivers. The design layout prioritized accurate and seamless characterization after front-end fabrication. Wafer assembly targeted matching the photonics to functional EICs to maximize the yield of functional co-integrated E-PICs. The design was taped out and the wafer was assembled with more than 20 design variations, while fabrication is on-going. It features a separation of 300 µm between the UTC-PD and driver input, mainly resulting from incorporating an on-chip resistor integrated along the CPW line and placed in between active devices. The separation can be potentially reduced to <15 µm for further scalability. Additionally, emphasis was placed on the need for a joint PDK and compact E-PIC models to achieve full design freedom and enable scalable and manufacturable 3D E-PICs in the future.

9.2 Perspectives

This section provides an outlook into the future developments of technologies used in this work. It is divided into three subject areas. The first part focuses on developments

concerning 3D integration. The second part focuses on the specifics of IMOS devices to improve their performance. The final part shifts the focus to enabling PICs and E-PICs that are compatible with the emerging packaging trends.

9.2.1 3D integration

The 3D integration methodology used in this thesis is not restricted to the IMOS platform. In theory, it is also possible to use a similar approach to integrate other PIC and EIC platforms as well. This is to either cover another wavelength spectrum range or to target other applications that require functionalities beyond the capacity of III-V materials. For instance, it could be possible to introduce low loss anneal-free SiN into the photonics layer on top of the InP to deliver better passive functionalities, including lower losses and higher Q resonators [228]. The same goes for using other materials like thin-film lithium niobate on SiN to enable high-speed modulators (>100 GHz) and nonlinear optical applications. It is also possible to tune III-V materials to target the visible wavelength range instead of IR as examples [229].

Thermal management will be crucial for the 3D E-PIC devices functionality and energy efficiency. BCB is ideal for low thermal crosstalk between electronics and photonics. The co-design rules set here were based on simulations to enable functional co-integrated devices with low thermal crosstalk. These effects could be tested by placing thermal-sensitive elements close to electronics and assessing the influence of this *vs* distance. Moreover, the full 3D E-PIC footprint obtained from simulation can be accurately assessed using advanced thermal imaging techniques to accurately map hotspots, such as thermo-reflectance microscopy [230], [231].

Bonding with BCB anchors has proven to be effective for better alignment accuracy and bond uniformity. The latter shows that it is possible to consistently achieve good alignment accuracy and bond uniformity. However, this was only tested for a BCB anchors density of 20% relative to the area reserved for soft-baked BCB. As it was shown, the anchors can be placed anywhere with no physical restrictions, which signifies that the density can be further increased. The latter results in higher anchor-to-bond BCB volume ratio, hence possibly achieving better performance. Moreover, anchors here were fabricated using lithography and dry etching, whereas these can also be realized using photo-definable BCB. This should be tested as it reduces the processing steps and time.

The technology developed here is based on InP-on-InP bonding, so it scales with the InP wafer size that is currently at 6 inch. Integrating membrane nanophotonics on SiGe BiCMOS EICs offers more scalability. Si substrates as large as 300mm are available. Co-integration of InP nanophotonics with these substrates can be realized via the smart cut process [232]. Here, several InP wafers are cut into dies and stacked in an array onto the large Si substrate to cover its full area. After bonding, epi-growth of InP-based active stacks and/or direct fabrication of active devices is possible.

Finally, co-design of the 3D E-PIC demonstrator relied on adapting the design of photonics to the electronics layout. However, unlocking the full potential of 3D integrated E-PICs is only possible if the chip is treated as a single system, thereby optimizing each device within the specification of that system. This implies using a unified compact simulation model that includes PIC devices, EIC drivers, and the TPV interconnects. Additionally, a joint PDK needs to be developed. By respecting the co-design rules, optimal placement of electronic and photonic devices could be realized to maximize the performance and reduce the footprint. To note, implementing GCs with

back reflectors is ideal here to retain the full design freedom of the chip optical I/O locations and lower insertion losses [68].

9.2.2 IMOS platform development

Various IMOS devices were further developed within this work. However, this raised a lot of open questions that require further investigation to bring their full potential to fruition. Specific developments for each device type are put together in their own sub-section, while some of the general remarks are provided here.

To increase the throughput, fabrication of membrane devices and post-bond 3D integration processes must rely on DUV scanner lithography instead of EBL. Quantifying spatial distortions resulting from bonding indicated that this is possible. Most wafers bonded with BCB have linear expansion as the dominant distortion. Pre-compensating that in scanner reticles should enable post-bonding lithography. Moreover, all distortions besides linear expansion are less significant and can be corrected for by the scanner. This indicates that the same pre-compensated reticle can be used for multiple wafers, provided that these wafers do not have any detrimental defects that significantly affect distortion. Moreover, enabling scanner lithography for post-bonding processing should improve the sidewall roughness of passive waveguides as well as the SOA active mesa sidewall [68]. This can lower the propagation losses to enable more complex circuits. In addition, all other steps that are realized with EBL and do not require very low tolerances could be transferred to direct laser writing instead. The writing time of this tool is an order of magnitude faster than EBL, and it provides a resolution in the order of 400nm.

For active IMOS devices, it was shown that thick plated Au is necessary for membrane active devices for better thermal dissipation and lower RF losses. Improved performance was shown for SOAs and UTC-PDs, while EAMs that are in the development phase also use thick plated Au. The latter is also beneficial for packaging using wire bonding or flip-chip solder bumping compared to thin Au, as it reinforces adhesion. However, phase shifters on IMOS benefit from the localized heating granted by BCB. So these might require using thin Au. In that case, the lift-off Au could be realized after plating to avoid damaging it during the seed layer wet etch.

SOAs and DFB lasers

The net gain and transparency current of C-band MQW SOAs for different shunt configurations was not measured. Structures for this measurement were fabricated in the same run, so these can be measured in the future to fully compare the effect of shunting only one contact side to both sides.

Further improvements on the thermal shunt could be realized by reducing the thermal dissipation path distance between the MQW core and the Si substrate as well as by bringing the metal closer to the core without compromising on the optical losses [172]. Final metallization plating for DFBs was realized via proximity lithography and took into account the worst-case-scenario in terms of membrane distortions. The distance of the path could be effectively reduced from 12µm to 2-3µm by the available tolerances granted by EBL or laser writing. Simulations in Annex A show that reducing this path distance, along with reducing the substrate thickness via wafer thinning could result in substantial improvements. The normalized thermal resistance could be lowered to 0.0295 K.m/W, which is among the state-of-the-art of heterogeneously

integrated lasers on Si. Further processing improvements were also discussed and could bring more benefits to thermal dissipation.

Beyond single device fabrication improvements, the density scaling potential of thermally shunted SOAs/DFBs can open doors to various applications such as compact transmitters and optical phased arrays. An array of 8 thermally shunted DFBs was fabricated in the same laser run realized within Chapter 6, but it requires wire bonding to turn on all DFBs at once, so it was not possible to measure within the timeframe of this work. The total array width is around 800μm, while another design using the similar shunt design achieves 400μm width. It is possible to decrease the width even further to reach the fundamental limits of the butt-joint regrowth [233]. Here, complex circuits could be realized with selective-area regrowth to enable compact DFBs with similar characteristics and operating at different wavelengths for the transmitter. Both DMLs and EMLs could benefit from this technology. Moreover, reducing the insertion losses within the SOA could be achieved by replacing twin-guide tapers with butt-joint tapers [174].

UTC PDs

The dark current of PDs with thick pads was measured, showing a leakage path for shunted PDs but also a plausible improvement due to lower thermal effects. Further investigations into these thermal effects on the dark current are thus required. The best external responsivity of shunted PDs is 0.46 A/W at -4V for PD with area of $2.92\times3\mu m^2$. This could be further improved by integrating these UTC-PDs with booster SOAs. The latter is either realized via a regrowth step, or the epi-stack of the UTC-PD can be flipped and integrated with the SOA stack below the passive waveguiding layer. The second option requires no regrowth so it is more favorable in terms of fabrication [105].

As discussed, an I_{max} value of 9.1mA was achieved for a single PD with dual injection and thick metallization. Further improving the optical field distribution uniformity within the PD and using 5μm thick Au could enable better power handling. I_{max} could be further boosted by employing circuit-level solutions utilizing these PDs in an optically parallel configuration and sharing the same CPW line. The bandwidth of UTC PDs on IMOS is not RC limited, so these devices can be scaled to higher bandwidths. Moreover, for circuit-level solutions targeting better power handling, the short CPW length requires no termination resistors. This indicates that the bandwidth of these solutions is scalable with the bandwidth of standalone PDs. High RF power at high bandwidths could enable applications such as mm-wave generation and TIA-less receivers. To note, the absolute RF power of single and circuit-level UTC-PDs was not measured within this thesis. This is a crucial parameter to quantify and define further improvements for devices targeting these applications.

For both UTC-PDs and lasers, the currently used passivation method is not ideal. It relies on SiO_2 deposited via PECVD at 300°C, and the deposition is highly directional, so sidewall passivation is not fully achieved. Using ALD for high conformal coverage and low damage is better. In this case, thermal ALD recipes are more preferred compared to plasma recipes [234]. However, wet chemical passivation with Ammonium Sulfide $(NH_4)_2S$ or other solutions yields the most optimal conditions for passivation in any case [235]. So this can be combined with thermal ALD Al_2O_3/SiO_2 for full and long-lasting surface passivation of dangling bonds.

9.2.3 Packaging

For efficient active cooling of 3D E-PICs from the electronics substrate, it is shown in Annex B that the substrate thickness plays a big role. Hence, reducing its thickness via wafer thinning is crucial before dicing. The minimum possible thickness is around 0.15mm for InP. Figure 9.1 shows the envisaged packaging methodology for TWILIGHT devices, whereby the E-PIC chip is flip-chip solder-bumped into an interposer and the TEC cools the EIC side. Instead, active cooling from the top of the membrane could be very effective to directly remove the heat from the photonic devices. This could be realized by using advanced packaging schemes, such as using a glass or Si interposer featuring TSVs, and connecting the other side of the interposer to a second TEC [236]. With that, both top-side active cooling from the photonics and bottom-side cooling from the electronics could be achieved. Cooling the electronics might not be necessary in that case, but this would require another estimation of the maximum chip temperature and a re-evaluation of the thermal crosstalk co-design rules. Moreover, it was shown in Chapter 2 that the thickness of the membrane on top influences heat spreading. Thus, it is possible that using heat spreaders on top of the membrane could be a useful way to further dissipate the heat towards the active cooling element. This combined with plated Au and advanced strategies to remove the heat locally from hot spots could close the gap between membrane and generic PIC devices in terms of thermal performance.

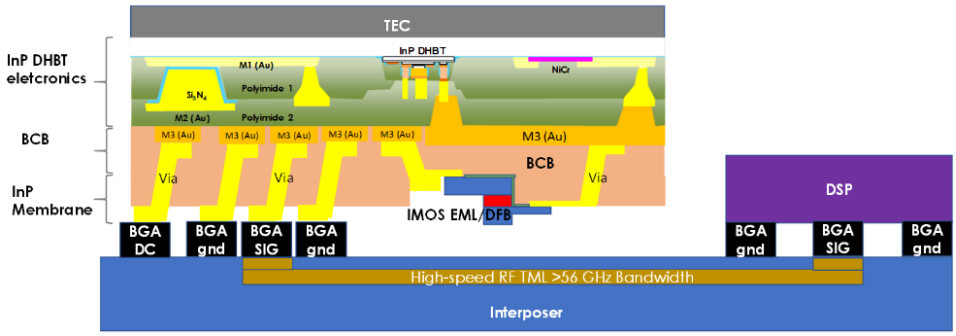

Figure 9.1 cross-section of the co-integrated E-PIC on the interposer, taken from [20]

Note that efficient heat sinking for 3D E-PICs is a common issue with vertically stacked EIC chiplets [99]. Thus potential solutions proposed for the latter could also apply to 3D E-PICs. For instance, it might be possible to consider fabricating structures that act as microfluidic cooling channels within the bonding BCB to locally cool hotspots. This is already being investigated on EIC chips having dense hotspots [237], [238]. Another aspect is to use localized micro-TECs surrounding hot spot areas and shielding areas having very low tolerances to thermal crosstalk [190].

I/O SSCs will be crucial for the photonics platform. These are needed for lower optical coupling losses and polarization insensitivity. More importantly, edge coupling devices are easier to package compared to vertical coupling at an angle, so these are compatible with emerging packaging standards. Also, vertical coupling cannot be realized if double-side active cooling is implemented, so SSCs would be the only solution here. Finally, the discussed strategies could help in establishing packaging standards at an early stage of the E-PICs development. This helps in aligning E-PICs development with the capabilities of the packaging industry based on similar technologies such as 2.5D integration, and targeting packaging for specific applications like CPO.

A

Appendix A

10.1 E-beam metrology and membrane distortions

10.1.1 Values of linear and residual distortions for all experiments

Table 0.1 Fitting results for all experiments

Sample Nr.	BCB thickness (μm)	Substrate material	Other notes	x-scale (ppm)	y-scale (ppm)	Non-orthogonality (Rad)	StDev (nm)
1	1	Si	lot of e-beam drift from long exposure	316.85	303.86	$1.52.10^{-4}$	151.15
2	1		/	321.6	306.95	$2.34.10^{-4}$	109.58
3	1		/	314.05	306.6	$8.21.10^{-5}$	102.34
4	2		/	319.76	309.92	$2.32.10^{-4}$	56.06
5	2		/	317.58	306.95	$8.36.10^{-5}$	112.90
6	2		/	318.48	307.26	$7.93.10^{-5}$	113.14
7	2		bonding with 90° Angle	325.11	317.74	$1.66.10^{-6}$	123.47
12	2		Cracked wafer left side	313.83	329.7	$9.81.10^{-6}$	125.90
	2		Cracked wafer right side	312.88	318.52	$3.63.10^{-6}$	73.57
8	12		/	323.46	322.91	$1.14.10^{-6}$	104.26
9	12		/	319.19	318.71	$6.13.10^{-6}$	116.42
10	12		positive markers (no InP membrane)	326.62	315.94	$3.11.10^{-6}$	132.63
11	12		Diced (bottom half)	-0.35	4.55	$7.78.10^{-6}$	43.67
	12		Diced (top left)	1.01	0.42	$5.03.10^{-6}$	40.75
	12		Diced (top right)	1.69	3.55	$6.07.10^{-6}$	16.24
13	2	InP	/	7.1	1.96	$1.10.10^{-4}$	60.84
14	2	SiC	/	320.64	313.45	$1.23.10^{-5}$	87.78

10.1.2 Evaluation of the accuracy from EBL and the model

In this section, we aim to understand the effect of EBL settings on the STDev of fitting errors during marker reading/writing. All of the experiments were done on InP

substrates. The main errors that arise from EBL are related to the beam drift and used beam current. Beam drift arises from temperature fluctuations <0.1 °C of the chamber [152]. It can particularly affect results for large writing time and field areas like writing on the wafer scale of a 3-inch wafer. Beam drift is corrected periodically by EBL each 1h, but values in-between are not possible to correct for. Secondly, increasing the beam current leads to a higher beam diameter, as identical markers will have a difference in marker image contrast and edge sharpness for different currents, thereby affecting the registered marker positions on the nanometer scale during metrology. For the experiments, we note that apart from the comparison between the effect of spatial map resolutions on errors, all results presented here use coarse maps with ~100 markers since this is the typical resolution close to functional photonics fabrication runs.

A

First, we assessed the effect of beam drift and current on marker lithography and metrology without using the fitting model. We note that the exposure time for the full map is around 10 minutes. An identical map with a 675 µm x-shift from the other map was also fabricated on the same wafer and designed to be exposed in 60 minutes, corresponding to the typical time required for full marker fabrication during a functional photonics run. These maps were then read multiple times with multiple beam currents without loading/unloading the holder. Next, marker positions were extracted from different reading times and fitted where both (x, y), and (x_0, y_0) described in section II are positions of the same marker, but read at a different time. Here, no distortions are present and only EBL reading accuracy is fully assessed, and systematic EBL errors are extracted. We first calculated the STDev of errors in nm *vs* current and their corresponding bell plots and results are shown in Figure 0..a and .b. We note that using 100 markers is sufficient to describe the distribution of errors in a Gaussian manner. Here, STDev is below 5 nm for beam currents below 100 nA and ~8.5 nm for a beam current of 190 nA. This is directly related to the increase in beam diameter. Increasing the markers' exposure time from 10 to 60 minutes during fabrication does not increase the STDev above 1nm. Moreover, the difference in STDev between different spatial map resolutions (not shown) is below 2 nm, which signifies that EBL-related systematic errors are similar for different map resolutions. Hence, it is possible to use resolutions close to that of coarse maps to accumulate accurate data on the distortion of InP membranes. The difference in markers' position from two different reading sessions extracted using a 5 nA beam is shown in Figure 0..c. Here, the vector directions are random and do not show any wafer-scale trend, signifying that these errors are intrinsic to the EBL reading accuracy, and hence cannot be corrected. Similar values were obtained from other e-beam metrology studies [143].

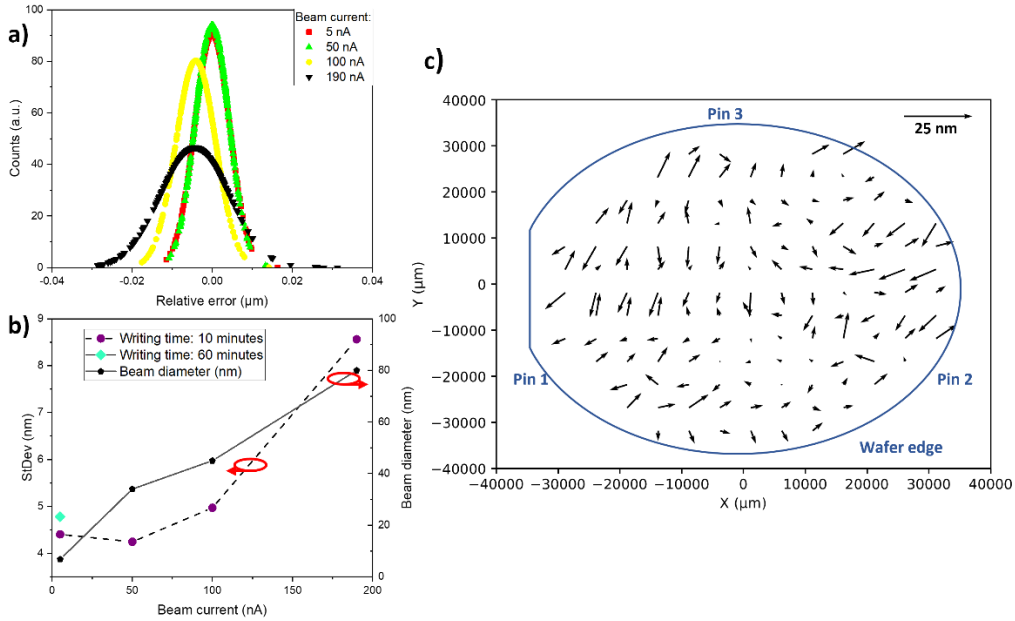

Figure 0.1. a) Bell plots representing the distribution of marker reading errors for different beam currents. b) STDev of errors and beam diameter *vs* beam current. c) Difference of markers position read at two different times using 5nA beam showcasing the effect of beam drift.

Next, we assessed the accuracy of our model based on these findings. Here, we compared the found marker positions with the designed positions and extracted the six distortion parameters based on Eq.(3) and Eq.(4). Given the non-systematic nature of drift as an error source, we also compared single datapoint-per-marker maps with averaged ten datapoints-per-marker maps. The resulting fitted parameters and standard deviations are summarized in Table 0.2. We ignore P_1-P_3 as these depend on the initial positioning of the wafer, these values are indeed similar to the values that EBL shows in the log. The reading accuracy increases by averaging the data, as shown by comparing the STDev values in Table 0.2. Based on the comparison of STDev values presented in Table 0.2, we conclude that using smaller beams (low beam current) and averaging the data from several readings of the same marker slightly increases the accuracy of results.

Bell plots representing the distribution of marker displacement based on the averaged data *vs* different currents are shown in the inset of Figure 0.. The distortion map extracted with 5 nA beam is shown in Figure 0. as well. Here, a wafer-scale trend is evident where the largest vectors lie on the edges of the wafer, and the markers near pin 1 have the largest displacement. We note that this is consistent in all of our extracted maps both on InP and from bonded membranes, suggesting that such deformations result from stresses exerted by the metal pins used to clamp the wafer to the holder. Rotating the wafer 90° with respect to the holder and reading again results in the same pattern near the pins (Figure 0.). Hence, these are likely not be permanent deformations. On the other hand, the difference in values between P_4 and P_5 is permanent because their values swap for the rotated wafer compared to the values

shown in Table 0.2. Here P_4 is 0.728 ppm and P_5 is 4.245 ppm after rotation. This difference is most likely resulting from the difference in bow between the two directions in the InP wafer, so the partial neutralization of the bow by the holder results in higher displacements in one direction relative to the other during marker writing. Finally, by comparison of the bell plots in Figure 0., the reading errors are similar for similar beam currents in this case, as the errors arising from marker displacements characterized by the pattern in Figure 0. dominate the STDev of errors.

A

Table 0.2 Distortion model parameters extracted for different currents and different number of data points per marker

Current, (nA)	Beam diameter (nm)	DataPt per marker	Reading time per map (second)	P_4 (ppm)	P_5 (ppm)	P_6 ($.10^{-07}$ Rad)	STDev (nm)
5	6.8	1	758	3.058	1.386	6.27	19.032
5	6.8	>10	758	3.148	1.363	7.25	18.355
50	25.0	>10	696	3.304	1.646	5.81	18.355
100	50.0	>10	695	3.559	1.577	3.23	18.900
190	80.0	>10	703	4.011	2.354	4.98	19.229

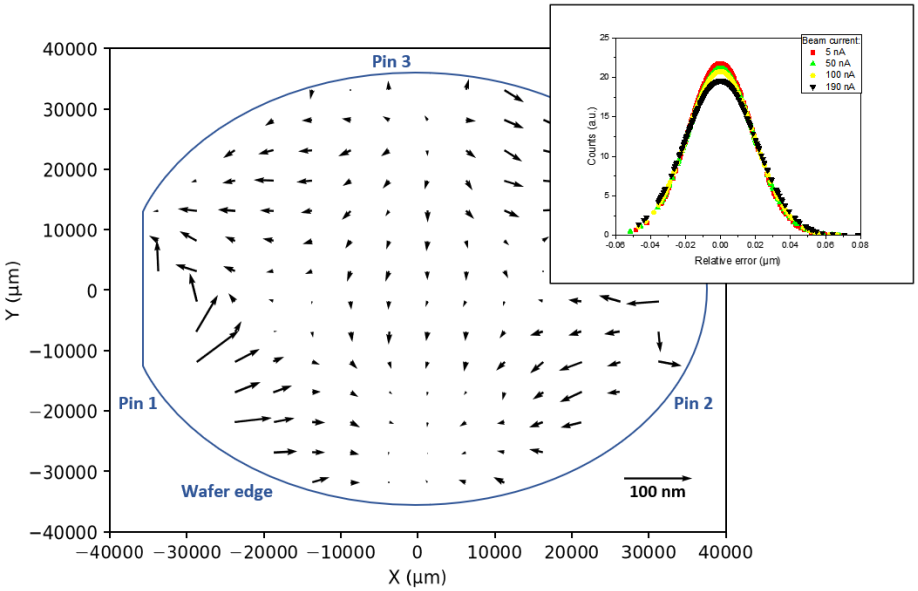

Figure 0.2. Difference between expected (design) and observed marker coordinates after removal of linear distortions, inset: bell plots showing fitting errors *vs* different beam currents after fitting to design coordinates

10.1.3 Bonding with a 90° angle between InP and Si

An image and distortion map of the InP membrane bonded onto Si with a 90° angle are shown in Figure 0..a and .b, respectively. The bonding interface is uniform and similar to other experiments, indicating that the rotation does not introduce defects due to the mismatch in the wafer flats. The overall residual distortions in Figure 0..b are higher

than in other experiments (see the scale), and the effect of pins on the distortions near the edge is not clear, indicating that these are exacerbated since marker fabrication and reading are done at two different angles.

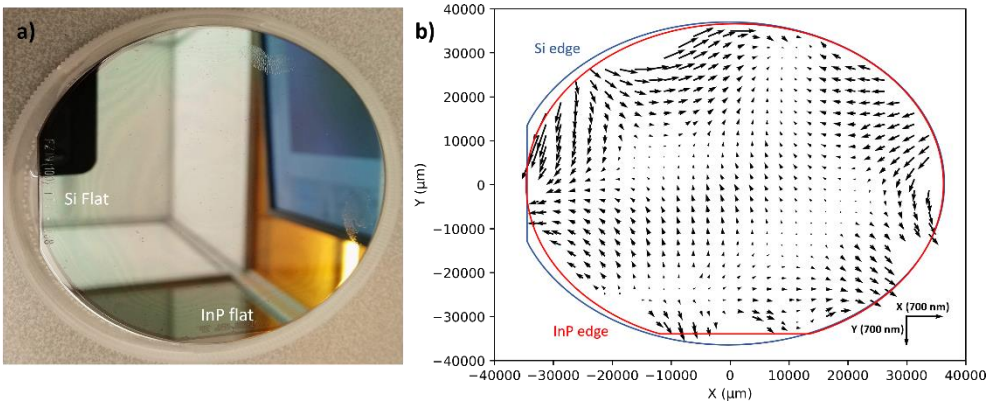

Figure 0.3. InP membrane bonded with 90° rotation with respect to the Si carrier: a) post-bond image, b) post-bond distortion map

B

Appendix B

10.2 Additional results related to shunted lasers

10.2.1 Resistance of shunted devices

To improve the thermal dissipation of the IMOS laser, the effective thermal connection distance between the laser core and Si substrate needs to be short. However, as mentioned in Chapter 5, the laser contacts are fabricated before bonding and then accessed by opening the semiconductor after bonding. This indicates that a minimum overlap between the semiconductor and ohmic metal contact is required for efficient current injection. To evaluate the overlap, the resistances of 0.5mm- and 0.75mm-long devices were measured for different overlap values between the semiconductor and metal contact. The chosen overlap range is 6 to 25 μm, and covers both shunted and reference device parameters for the overlap. Note that the overlap between the contact metal and 5μm-thick Au for this test was fixed at 6μm to ensure all DFBs are properly connected on the wafer scale. Figure 0..a) shows the resistance values between devices with different semiconductor-metal overlaps in the range of 6-26 μm for DFB lengths of 0.5mm and 0.75mm. It can be seen that for both lengths the resistance is almost constant in the range of 7-6.5 and 5.8-5.6 Ω for laser lengths of 0.5mm and 0.75mm, respectively. This indicates that a lower overlap can be used without deteriorating the device electrical performance. So further improvements based on the next section are possible.

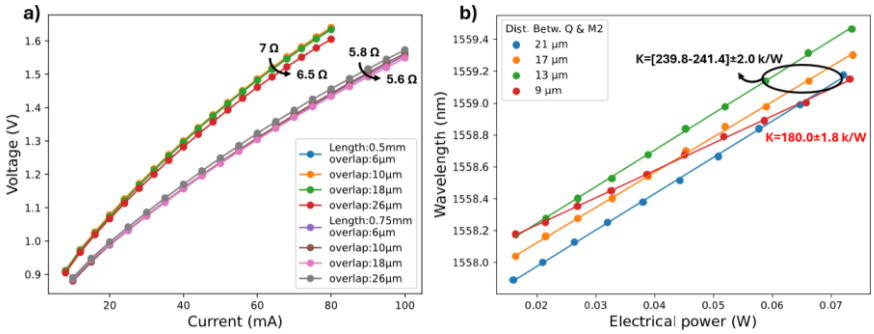

Figure 0.4 a) I-V curves for 0.5 and 0.75mm-long DFB devices with different metal semiconductor overlap. b) Wavelength shift *vs* electrical power for 0.5mm-long DFBs and varying distance between the heat source (Q) and shunt metal

10.2.2 Effect of varying the distance between the shunt and active core

Secondly, we studied how the distance between 5µm-thick Au shunt and active core mesa affects R_{th}. For this, the width of the initial contact metal that is made before bonding is fixed at 30µm, while the overlap between this metal and the semiconductor was fixed at 6 µm. The shunt distance is then varied at distances away from the mesa in the range of 9-21µm. The wavelength shift *vs* power for 0.5mm-long DFBs in this study are shown in Figure 0..b. The thermal resistance for devices with a 9µm distance is 180.0±1.8 K/W. Further increasing the distance to values between 13 and 21µm resulted in higher R_{th} values in the range of 239.8-241.4±2.0 K/W. This indicates that this distance needs to be as small as possible to decrease the temperature of the core, while further increasing the distance means that the shunt only dissipates part of the heat that has spread out through the thin metal contact to the substrate. This is consistent with simulation results shown in Figure 0..d

10.2.3 Further improvements to the thermal shunt

Figure 0. shows several possible improvements of the DFB thermal shunt structure without introducing new materials or altering the process flow. In Figure 0..a), we investigated using 200nm thicker initial p- and n-contact metals, which is possible during the same contact metal lithography via lift-off. However, the latter decreases R_{th} of shunted devices by only 8-10 K/W depending on the shunt thickness and for all studied BCB thicknesses. This represents around 6% improvement compared to the default configuration used in the body of the paper. However, R_{th} decreases by at least 40 K/W (≈12%) for reference isolated devices. This is because thicker Au helps in laterally spreading the heat to the sides of the DFB.

The effect of substrate thickness is shown in Figure 0..b). A reduction of R_{th} by≈20 K/W can be achieved for each 100µm reduction in Si substrate thickness. This is because the heat dissipates vertically through the substrate towards the heat sink. Thus, the thinner the substrate, better the heat dissipation. Moreover, for all configurations, using InP substrates imposes ≈35 K/W higher R_{th} relative to Si, while using SiC substrates reduces R_{th} by ≈25 K/W relative to Si, which is linked to the thermal conductivity difference between these substrates. The thermal resistance of devices on InP and SiC are found in Figure 0..a) and .b), respectively.

The overlap between the thermal shunt and the initial metal contact could also be reduced from 6µm to 1µm with better overlay lithography tools but gives no significant effect for thick shunts. Figure 0..c) shows the potential of this change. It can be seen that an overall improvement in R_{th} is only seen for vias thicknesses below 1µm, while R_{th} for devices with 2.5-5µm shunt is only reduced by 3-5 K/W.

Finally, Figure 0..d) shows the impact of bringing the shunt metal closer to the DFB mesa sidewall. This improvement is possible because the electrical transfer length is in the order of 1-2µm, so etching the semiconductor for contact opening at these sizes is possible without affecting the current injection efficiency. This improvement is much more important for thick vias >1µm. Here, R_{th} can be lowered by an additional ≈25% for all BCB thicknesses.

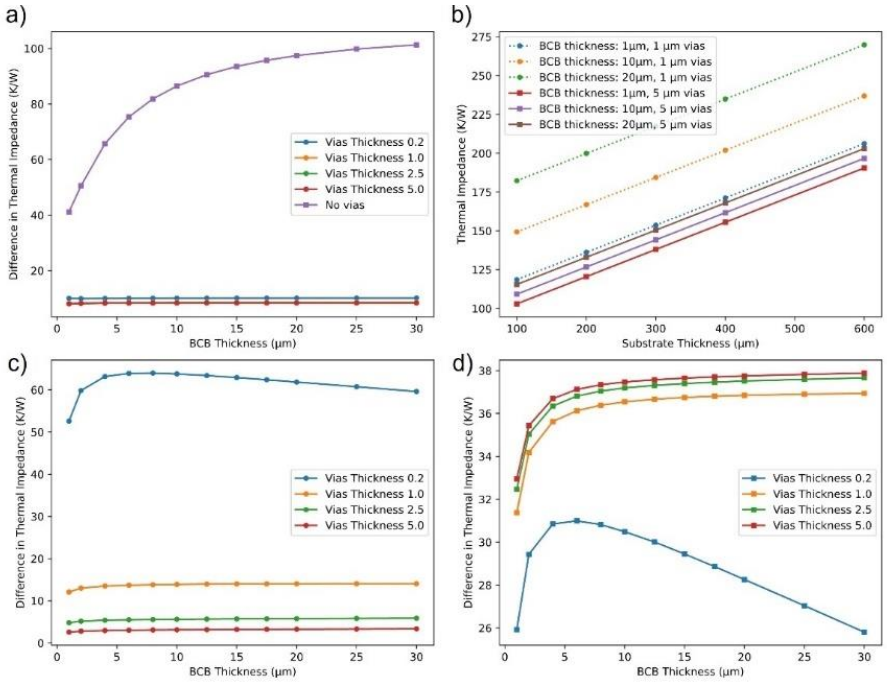

Figure 0.5 Simulated R_{th} reduction for 500µm long DFBs with/without thermal shunt showing the impact of: a) using thicker contact Au for n- and p-contacts *vs* BCB thickness, b) substrate thickness, c) lowering the overlap between the Au shunt and contact metal from 6 to 1µm, d) lowering the distance between the DFB mesa and shunt start from 6µm to 1µm

By implementing all of these improvements discussed earlier, the thermal resistance of shunted devices at 2µm BCB can be reduced from 149 K/W to 59 K/W, *i.e.*, normalized R_{th} of 0.0295 K.m/W) without influencing the optical losses of the diode, which matches the state-of-the-art heterogeneous III-V devices on Silicon [173].

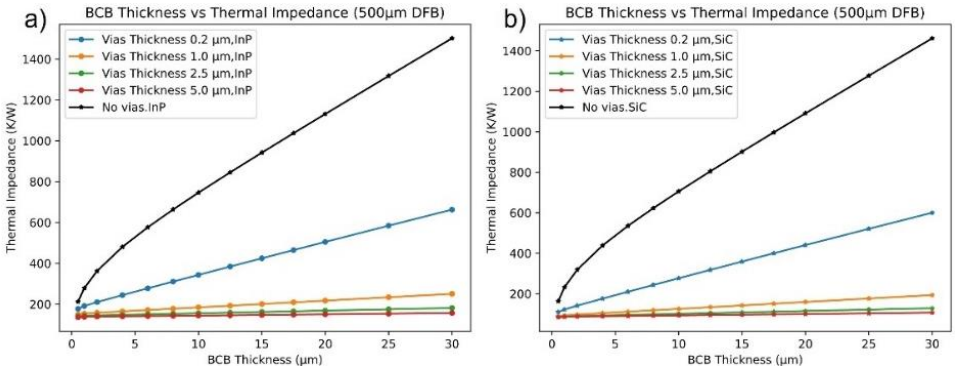

Figure 0.6 Simulated thermal resistance reduction for 500µm long DFBs on: a) InP substrate, b) SiC substrate

10.2.4 WPE of the 0.75mm-long DFB

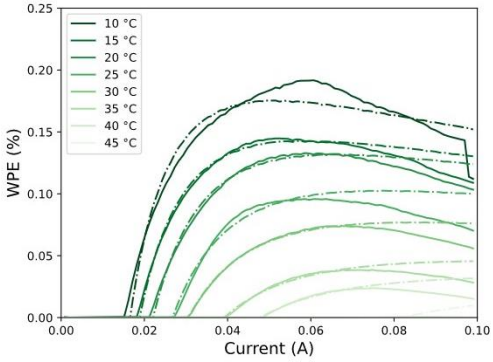

Figure 0.7 Wall plug efficiency of the 0.75mm shunted DFBs compensated for passive losses

The WPE of the 0.75 mm-long DFB is shown in Figure 0.. The deviation of the experimental curve from the simulated curve at 10°C between 40-60mA could be due to high-order effects such as two-photon absorption that cause additional losses in the passive section at these power values in the waveguide [239].

List of Abbreviations

2D	2-dimensional
2.5D	2.5-dimensional
3D	3-dimensional
ADeMUX	Analog demultiplexer
AI	Artificial Intelligence
Al_2O_3	Aluminum oxide
ALD	Atomic layer deposition
AlN	Aluminum nitride
AMUX	Analog multiplexer
ArF	Argon fluoride
ASIC	Application-specific integrated circuit
AWG	Arrayed waveguide grating
BB	Building block
BCB	Benzocyclobutene
BFGS	Broyden, Fletcher, Goldfarb, and Shanno
BH	Buried heterostructure
BiCMOS	Bipolar complementary metal oxide semiconductor
CMOS	Complementary metal oxide semiconductor
CPO	Co-packaged optics
CPW	Coplanar waveguide
CTE	Coefficient of thermal expansion
CTLM	Circular transmission line method
CW	Continuous-wave
DFB	Distributed feedback laser
DHBT	Double heterojunction bipolar transistors
DHS	Double heterostructure
DML	Directly-modulated laser
DRC	Design rule check
DSP	Digital signal processing
DUT	Device under test
DUV	Deep ultra-violet
E-PIC	Electronic-photonic integrated circuit
EAM	Electro-absorption modulator

EBL	E-beam lithography
EDFA	Erbium-doped fiber amplifier
EIC	Electronic integrated circuit
EML	Externally-modulated laser
FDTD	Finite-Difference Time-Domain
GC	Grating coupler
GDS	Graphic design system
GSG	Ground-signal-ground
HCl	Hydrogen chloride
HEMT	High electron mobility transistors
HH	Heavy hole
HR-STEM	High-resolution scanning transmission electron microscopy
ICP	Inductively-coupled plasma
I/O	Input/output
IMOS	Indium phosphide membrane on silicon
InP	Indium phosphide
IR	Infrared
KCN	Potassium Cyanide
LH	Light hole
LIV	Light-current-voltage
LP-MOVPE	Low-pressure metalorganic vapor phase epitaxy
ML	Machine learning
MMI	Multi-mode interference
MPW	Multi-project wafer
MQW	Multi-quantum well
MSE	Mean squared error
MZI	Mach-Zender-interferometer
$(NH_4)_2HPO_4$	di-Ammonium hydrogen phosphate
$(NH_4)_2S$	Ammonium sulfide
n.i.d.	Non-intentionally-doped
NIR	Near-infrared
OE	Optical-to-electrical
OSA	Optical spectrum analyzer
OSNR	Optical signal-to-noise ratio
PCB	Printed circuit board
PD	Photodiode
PDG	Polarization-dependent gain
PDK	Process design kit
PECVD	Plasma-enhanced chemical vapor deposition
PI	Polarization-insensitive
PIC	Photonic integrated circuit
PL	Photoluminescence
Ppm	Particle per million
RC	Resistor-capacitor
RDL	Redistribution layer
RF	Radio-frequency
RIE	Reactive ion etching
ROE	Run-out of error
RTA	Rapid thermal annealing
RT	Room temperature
Rx	Receiver
SCH	Separate confinement heterostructure
SEM	Scanning electron microscope

Si	Silicon
SiC	Silicon carbide
SiGe	Silicon germanium
SiO_2	Silicon oxide
SiP	System-in-package
SiPh	Silicon photonics
SMSR	Side-mode suppression ratio
SiN	Silicon nitride
SOA	Semiconductor optical amplifier
SoC	System-on-chip
SOLT	Short-open-load-thru
SSC	Spot-size converter
SR	Shallow ridge
SSC	Spot-size converted
STDev	Standard deviation
TE	Transverse electric
TEC	Thermo-electric cooler
TIA	Transimpedance amplifier
TM	Transverse magnetic
TPV	Through-polymer vias
TSV	Through-silicon vias
TTV	Total thickness variation
Tx	Transmitter
UTC	Uni-travelling carrier
VNA	Vector network analyzer
VOA	Variable optical attenuator
WDM	Wavelength division multiplexing
WPE	Wall-plug efficiency
XRD	X-ray diffraction

List of Publications

Journal articles

[J1] S. Abdi, J.de Graaf, et al, "Membrane UTC-PDs with improved power handling and RF power," 2025. To be submitted.

[J2] S. Abdi, K. Williams, and Y. Jiao, "Enhanced thermal dissipation for BCB-bonded 3D integrated membrane photonic circuits," *J. Phys. Photonics, vol. 7, no. 2, p. 025003*, Feb. 2025, doi: 10.1088/2515-7647/adaf63.

[J3] S.Reniers, Y.Wang, S. Abdi, J.de Graaf, A.Zozulia, K.Williams, and Y.Jiao, "Highly Versatile Photonic Integration Platform on an Indium Phosphide Membrane," 2024. To be submitted.

[J4] D.W. Feyisa, Z.Chen, S. Abdi, et al, "IMOS-Compatible Spot Size Converted for Low Loss, Broadband, and Low Polarization Dependent Loss Fiber-to-Chip Edge Coupling," 2024. To be submitted.

[J5] D.W. Feyisa, S. Abdi, Y. Jiao, N. Calabretta, and R. Stabile, "Scalable SOA-based Banyan optical space switch on InP membrane on silicon (IMOS)," *Opt. Express, vol. 32, no. 23, pp. 41948–41960*, Nov. 2024, doi: 10.1364/OE.538459.

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[J7] S. Abdi et al., "Research Toward Wafer-Scale 3D Integration of InP Membrane Photonics With InP Electronics," *IEEE Trans. Semicond. Manuf., pp. 1–1*, 2024, doi: 10.1109/TSM.2024.3382511.

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[J9] S. Abdi, T. de Vries, M. Spiegelberg, K. Williams, and Y. Jiao, "Novel wafer-scale adhesive bonding with improved alignment accuracy and bond uniformity," *Microelectron. Eng., vol. 270, p. 111936*, Feb. 2023, doi: 10.1016/j.mee.2023.111936.

Conference contributions

[C1] M. Spyropoulou...S. Abdi...*et al.* "InP photonics and InP-DHBT electronics co-integration for high capacity and scalable datacenter interconnect applications," 2025 IEEE Photonics Society Summer Topicals Meeting Series (SUM). Invited.

[C2] S. Abdi, J.de Graaf, K. Williams, and Y. Jiao "Enhanced Bandwidth and Power Handling in Heterogeneous UTC-PDs via Optimized Thermal Design," Compound Semiconductor Week (CSW) 2025. Accepted.

[C3] D.W. Feyisa, S. Abdi, et al "2×2 Optical Switch on an InP Membrane on a Silicon (IMOS) Platform for Modular Switching on Chip," 50th European Conference and Exhibition on Optical Communication – ECOC 2024, 22-26 September 2024.

[C4] S. Abdi, A. Zozulia, and Y. Jiao, "Thermal Management for Wafer-Scale Heterogeneously Integrated InP Lasers on BCB," in *2024 IEEE 29th International Semiconductor Laser Conference (ISLC)*, Sep. 2024, pp. 1–2. doi: 10.1109/ISLC57752.2024.10717400.

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[C6] M. Spyropoulou...S. Abdi...*et al.*, "The future of multi-terabit datacenter interconnects based on tight co-integration of photonics and electronics technologies," in *2023 Optical Fiber Communications Conference and Exhibition (OFC)*, Mar. 2023, pp. 1–3. doi: 10.1364/OFC.2023.Tu3I.3.

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[C12] D. W. Feyisa, Y. Jiao, S. Abdi, Z. Chen, N. Calabretta, and R. Stabile, "An O-band Polarization-Insensitive SOA Building Block for SOA-Based Optical Switches in IMOS Platform," in *25th annual Symposium of the IEEE Photonics Benelux Chapter*, Mons, Belgium, Nov. 2021.

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Patent

[P1] EU and US patent WO 2023/239238 A1: S. Abdi, T.de.Vries, and Y.Jiao, "A method for bonding a first and second planar substrate," PCT phase ended in Dec/2024, Applied for EU and US

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As I reach the final words of my thesis, I find myself facing what may be the most challenging section to write, the acknowledgments. This journey would not have been possible without the countless individuals who have left a mark on my personal and professional life. I deliberately saved this section for the last day before printing, knowing that no matter how carefully I try, I may still overlook someone. For that, I sincerely apologize.

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Biography

Salim Abdi was born in Medea, Algeria, in 1994. In 2018, he received a bachelor's degree in materials science from the Ecole National Polytechnique, Algeria, and in 2020, a master's degree in physics from the Ecole Polytechnique Montreal, Canada. During that period, he was rewarded a full scholarship from the Abdulla Al Ghurair Foundation for education to pursue his research. He focused on materials characterization, semiconductor physics, and fabrication of semiconductor devices. In 2021, Salim enrolled in a Ph.D. program in the field of photonic integrated circuits within the Photonic Integration Group at the Eindhoven University of Technology, The Netherlands. He focused on co-integrating InP electronics with InP membrane photonics to enable next-generation data communication modules. His research interests include materials development, semiconductor physics, electro-optic devices, heterogeneous integration, and systems-in-package.

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