

## Consortium



TU/e



Argotech



## MEET THE TEAM



6 partners



6 countries



3 Universities



2 Companies



1 Research Institute



PHOTONICS PUBLIC PRIVATE PARTNERSHIP



Project Title: Towards the neW era of 1.6 Tb/s System-InPackage transceivers for datacenter applications exploiting wafer-scale co-integration of InP membranes and InP-HBT electronics

Project Website: [www.ict-twilight.eu](http://www.ict-twilight.eu)

Project Coordinator: Hercules Avramopoulos  
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Duration: 01/12/2019 – 31/05/2024 (54 Months)

Partners: Institute of Communications and Computer Systems (GR) – Project Coordinator, Technische Universiteit Eindhoven (NL), III-V Lab (FR), Kungliga Tekniska Hogskolan (SE), Argotech (CZ), Mellanox Technologies (IL)

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Towards the neW era of 1.6 Tb/s System-InPackage transceivers for datacenter applications exploiting wafer-scale co-integration of InP membranes and InP-HBT electronics



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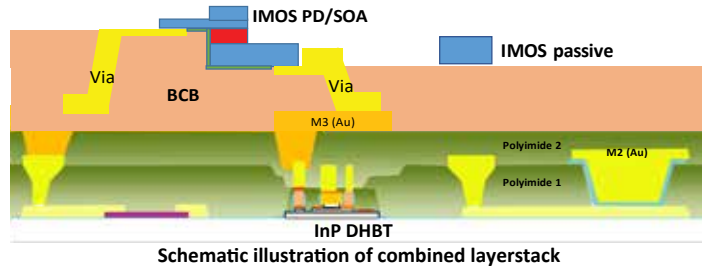


## The Vision

- ✓ To develop 100 Gbaud per wavelength co-packaged optical transceivers and optical space switches for next generation high speed datacenter interconnects.

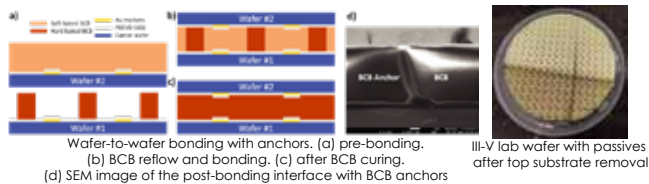
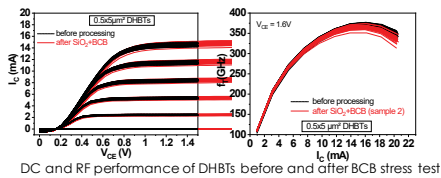
## Wafer-scale bonding of InP photonics & InP DHBT electronics ICs

- ▶ Ultra-short interconnects (~20µm RF vias) minimize high frequency RF parasitics
- ▶ Flexible optical and RF routing on the membrane chip
- ▶ High alignment accuracy between the two layers  
Minimum stress due to thermal mismatch  
Reliability in industrial environments

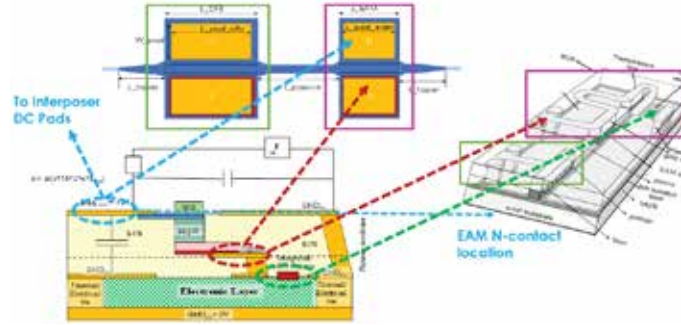


## Co-integration tests

- ▶ Wafer-to-wafer alignment bonding is done through SiN backside markers from the photonics wafer (±4µm)
- ▶ Novel wafer bonding using BCB anchors for high post-bond alignment accuracy
  - Average in-plane offset from different markers:
    - With no anchors: (24.6, 5.3)µm
    - With anchors: (8.2, 4.2) µm
    - With anchors on III-V lab wafer: (7.3, 5.8) µm
- ▶ DHBTs performance is preserved after BCB stress test

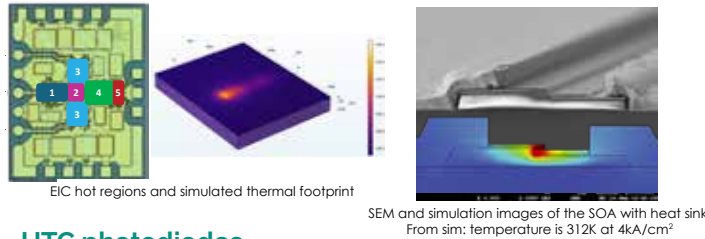


## DFB-EAM transverse cointegration schematic



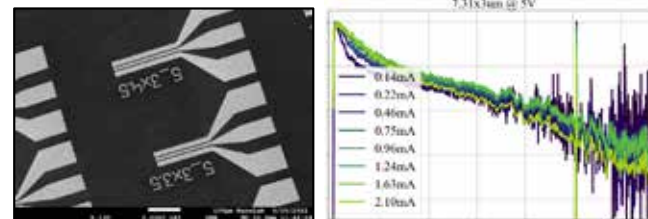
## Efficient heatsink for PICs bonded on EIC wafer

- ▶ The heat sink is based on >2µm plated Au
- ▶ Simulations show a reduction of at least 23°C between DFB lasers with/without heatsink
- ▶ This integration scheme is also compatible with high thickness BCB
- ▶ Thermal crosstalk between EICs and PICs can be reduced



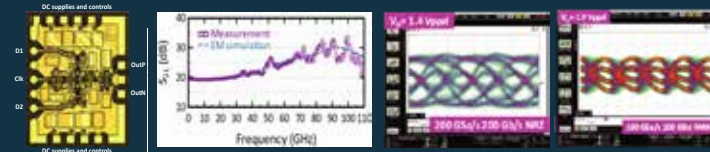
## UTC photodiodes

- ▶ Low dark current (<10nA) and high efficiency (0.6 A/W) in extremely compact photodiodes (typical footprint of 20 µm²)
- ▶ EO bandwidth as high as 60 GHz, with very low power dependence
- ▶ Total UTC-PD + 150pH bond wire+ TIA assembly has been simulated, showing 40 GHz overall bandwidth is feasible



## Newly developed III-V Lab InP DHBT process

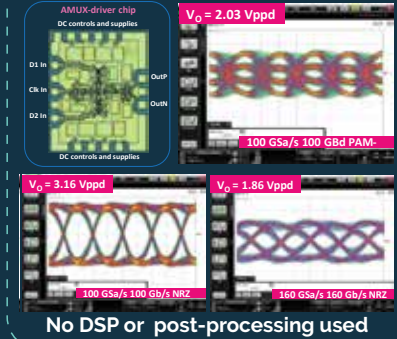
- ▶ **0.5-µm** DHBTs show **450/530 GHz**  $f_T/f_{MAX}$  with **> 4-V** breakdown voltage
- ▶ process allows the fabrication of **0.4 to 0.7 µm** emitter width DHBTs (> 99% DHBT yield)
- ▶ **200 GSa/s AMUX-driver IC** with >2.1-THz Gain×Bandwidth



## InP-HBT Transmitter IC

- ▶ Analog Multiplexing Driver monolithic IC (AMUX-driver)
- ▶ Linear driver with gain peaking at high frequency range functionality

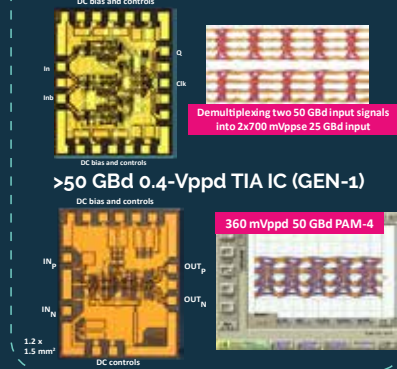
## >160 GSa/s >2-Vppd AMUX-driver IC



## InP-HBT Receiver ICs

- ▶ Analog Demultiplexing TIA IC (ADeMUX-TIA)
- ▶ Linear TIAs with:
  - Gain control
  - Bandwidth control
  - Output offset control
- ▶ Half rate clock signal for electrical de-multiplexing
- ▶ 2nd GEN ADeMUX and TIA in fab

## >50 GSa/s 0.7-Vppd ADeMUX IC (GEN-1)



## Impact

**TWILIGHT** comprises an industry-driven consortium and is committed to scale datacenter switch capacity beyond 102.4T leveraging more than 70% power consumption savings and cost 0.89€/Gb/s.