2×2 Optical Switch on an InP Membrane on a Silicon (IMOS) Platform for Modular Switching on Chip

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Abstract *We present the first optical switch integrated on InP membrane on the Silicon(IMOS) platform using SOAs with optimal OSNR and ER > 45 dB. NRZ-OOK routing shows 15 dB IPDR within 1 dB power penalty at 12.5Gb/s and power penalty of < 1.4dB at 40Gb/s. ©2024 The Author(s)*

Introduction

Optical interconnects have emerged as a practical solution to the scaling challenges modern dynamic data centres and supercomputers face [1], [2]. Google's recent adoption of optical circuit switches (OCS) in the architecture of its latest data centres is a testament to the practicality of this technology, a move particularly beneficial for AI/ML demands to minimize power consumption, latency, and heat generation [1]. Beyond traditional data centre applications, Google has also deployed a supercomputer with optical circuit switches implemented using 3D MEMS-based OCS [2]This setup allows for optical topology reconfiguration, enhances system resilience, reduces setup times through modular, incremental rack installation, and optimizes resource scheduling to boost utilization. These practical applications underscore the importance of further research on optical switches and their potential impact on data centre interconnects, demonstrating the tangible benefits and real-world impact of this technology.

While current applications primarily utilize MEMS-based switching technology, offering moderate switching speeds, future applications demand quicker alternatives due to latency considerations. Silicon photonics and semiconductor optical amplifier (SOA)-based switching technologies can both offer high speed [3], [4]. Silicon technologies can provide low-loss and compact devices, but amplification requires hybrid integration, which adds to the complexity. Generic InP enables monolithic integration of SOA-based switches, but the component size is large [5]. In contrast, implementing optical switch circuitry in InP membrane on a silicon (IMOS) platform offers a superior solution. This unique platform combines the best attributes of generic InP and silicon photonics, allowing for the integration of smaller waveguides, crossings, and bends than in its generic counterpart. This results in a more compact design while enabling the monolithic integration of active devices [6], [7], [8]. The SOA-based optical switch on the IMOS platform highlights the potential of IMOS in optical switch technology and outperforms existing SOA-based switching technologies in compactness, instilling confidence in the design of photonic integrated switch potential for future applications.

This paper introduces the first optical switch design in IMOS, a significant advancement in dense photonic integrated circuits for optical switch technology. Fabricated and characterized on the IMOS platform, this innovative switch offers a glimpse into the future of high-performance optical switches. The paper is structured as follows: First, we detail the fabrication process and switch circuit design. Then, we present the switch physical layer evaluation of a 2×2 switch module, including the loss measurements, extinction ratio (ER), and optical signal noise ratio (OSNR), crucial metrics in assessing the signal quality and performance of the switch. Next, we discuss data signal routing through the same switch module and determine performance via input power dynamic range (IPDR) and power penalty measurement. This first demonstration of a 2×2 switch module on the IMOS platform highlights the potential for significant advancements in optical switch technology, contributing towards data centre interconnects.

Platform, Switch Architecture and Design

Figure 1a provides the layer stack developed on the InP substrate after contact definition. Fig.1b provides a lateral view of the active and passive waveguide structure defined in the IMOS platform after bonding the patterned InP layer on top of the Silicon layer [8] via a BCB polymer layer. Specifically, the n- and p-contacts are shown in yellow colour. The active layer is made of InGaAs/Q for

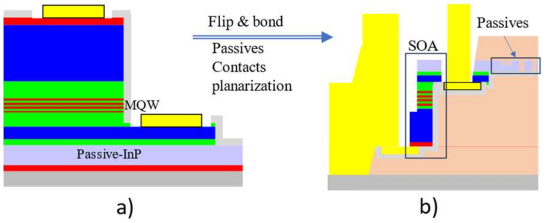

Fig. 1: a) Layer stack after active-passive etching and contact definition. b) Wafer bonding and substrate removal, passive definition, planarization, and final metallization.

the SOAs, and the passive InP layer is used to realize structures like waveguides, bents, couplers, and gratings. The SOA and passive structures are then passivated and the BCB is opened for the final metallization.

The performance of switches with limited ports relies on specific components, such as the SOA. These components are crucial in defining the switch's fundamental characteristics, including switching time, insertion loss, power consumption, and on/off ratio. Conversely, organizing the primary switch modules into modular architectures for switches with more ports is imperative. The most frequently utilized optical switches include the switch and select, Benes, close, and Banyan [4], [9], [10]. The design of optical switch architectures can significantly impact path loss, footprint, and blocking property due to variations in switching elements, stages, and crossovers. Ideally, a switch should offer lossless operation, high OSNR and ER, and a low BER. This study employs the Banyan architecture, a blocking design known for its compactness and fewer stages than other multistage switches. For N port counts, the architecture features two N/2 × N/2 switches in stages and an additional stage with N/2, 2×2 switches, a total of $\log2^N$ stages. When paired with the IMOS platform, the minimalist Banyan switch architecture produces a remarkably compact design, fitting an 8×8 switch in a 4 μm × 4 μm area. The future potential for densely integrated optical switches holds promise for even more compact designs with denser SOA pitch.

Physical Layer Measurement

A simple setup, shown in Figure 3a, is used to assess the switch's physical properties. The wafer is placed on a copper holder and kept at a temperature of 10 degrees Celsius using a water-cooling system. As seen in Figure 3b, two probes are used to bias the SOA at the required current. The input and output are coupled in and out via a grating coupler and cleaved single-mode Fibers.

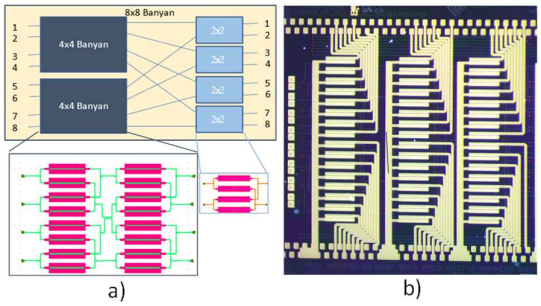

Fig. 2: a) 8×8 Banyan switch architecture constructed from 2×2 and 4×4 basic switches. b) Fabricated 8×8 Banyan optical switch.

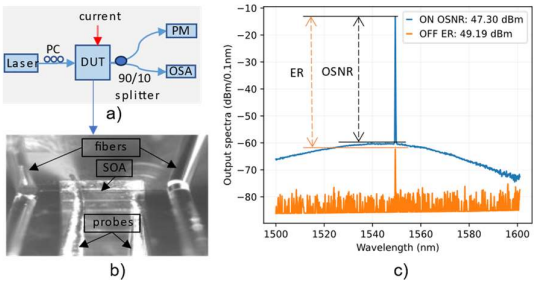

Fig. 3: a) Setup for spectral information analysis, b) device under test as seen in a microscope, c) ER and OSNR measurement.

A continuous wave signal is sent to the chip via a Polarization controller, which adjusts the Polarization of the light for optimal input to the chip, considering the polarization sensitivity of the SOA on the chip and the input/output grating coupler. Fig 3c shows a typical path OSNR and ER determined by comparing the output signal peak to the noise floor and OFF-state peak, respectively. We can see that the OFF-state output is less than the ON-state noise floor; hence, the crosstalk from another channel cannot affect the performance of the other. This setup allows for precise and accurate measurement of the switch's physical properties, providing valuable insights into its performance and capabilities.

Fig. 4 displays the switch output spectrum and associated OSNR and ER for wavelengths ranging from 1530 nm to 1560 nm in 5 nm increments. Four paths are measured: Path 1 (input one to output 1), Path 2 (input 1 to output 2), Path 3 (input 2 to output 1), and Path 4 (input 2 to output

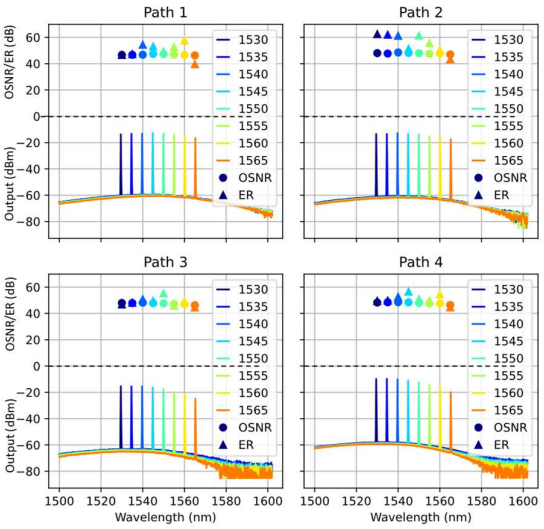

Fig. 4: Signal spectrum, extinction ratio, and optical signal-to-noise ratio for all basic 2×2 optical switch module paths. As shown in the legend, the colour codes show wavelength from 1530 nm to 1565 nm at step 5 nm. The dots and triangles represent OSNR and ER.

3), each illustrating the connection from specific inputs to outputs. With an input power of 6 dBm, the highest output recorded is -10 dBm, indicating a fiber-to-fiber loss of -16 dB. The measured loss attributable to the grating coupler is also -16 dB, suggesting that the 2×2 switch module is loss-less. The measured ER and OSNR values across all paths exceeded 40 dB for all the tested wavelengths. Path 2 had an ER of over 60 dB at a wavelength of 1545nm.

Data Signal Routing

The experimental setup for measuring data transmission on the switch is depicted in Fig 5a. A polarization controller feeds the laser light to the modulator to optimize the optical signal, then coupled to the chip with another polarization controller. Both polarization controllers are essential as the modulators in the transmitter assembly, and SOA on the chip is polarization dependent. After the switch, loss caused by grating couplers at both ends is compensated for by an Erbium-Doped Fiber Amplifier (EDFA). The modulated signal spectrum at the input and after being routed through the switch is shown in Figs 5b and 5c, respectively. The OSNR at the input and output are approximately 56 dB and 38 dB, respectively. The OSNR degradation after the switch is due to Amplified spontaneous emission (ASE) from the SOA and low input power. To evaluate the impact of the switch on signal quality, the power penalty is measured by comparing the sensitivity required to achieve a bit error ratio of 10^{-9} in data received directly (without the switch) to that passed through the switch.

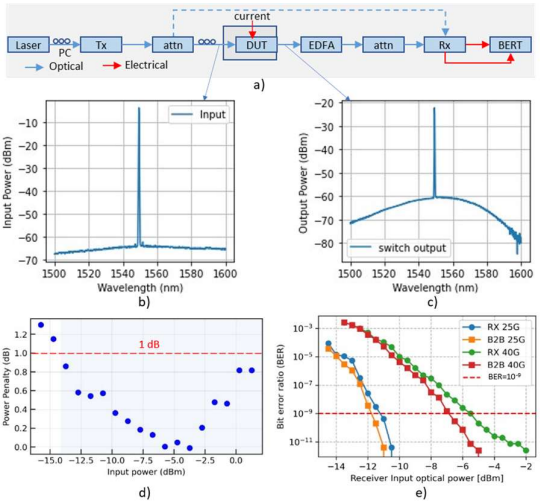

Fig. 5: a) Experimental setup for data transmission test b) transmitted signal spectrum at switch input c) Output signal spectrum after passing through switch d) Input power dynamic range (IPDR) measurement result e) Bit error ratio versus receiver input power for 25 GB/s and 40 Gb/s.

Fig. 5 (d) shows the power penalty measurement for different input powers at 12.5 Gbps to determine the input power dynamic range (IPDR). The bit rate of 12.5 Gbps is used since the current setup power budget does not allow IPDR measurements at 40 Gb/s. We measured a best-case error-free transmission with a power penalty of less than 0.3 and an IPDR of around 15 dB at a 1 dB power penalty, showing that the switch can tolerate the front-end power variation. The IPDR plot shows that the power penalty rises on the low- and high-power sides due to OSNR degradation (when power de-creases) and increasing non-linearity (when the power grows).

In Figure 5e, it is shown that when a 25 Gbps Non-Return-to-Zero On-Off Keying (NRZ-OOK) Pseudo Random Binary Sequence of length 31 (PRBS31) is transmitted through the switch, a power penalty of 0.8 dB is observed at a bit error ratio of 10-9. For a 40 Gbps transmission, the power penalty increases to 1.4 dB, and the power required for receiver sensitivity also increases.

Conclusion

This work shows the design and implementation of a highly compact SOA-based optical switch with a port count of up to 8×8 on the IMOS platform. The experimental results on the basic 2×2 switch module demonstrate excellent performance, with OSNR and ER exceeding 45 dB for continuous waves and greater than 38 dB for modulated signals passing through the IMOS SOA. The data signal routing shows minimal quality degradation, even at high speeds, as evidenced by a 1.4 dB power penalty with 40 Gb/s transmission. The switch can also adapt to varying input power, as shown by the IPDR measurement that reaches the 15 dB range with only a 1 dB power penalty at a data rate of 12.5 Gb/s. These encouraging results open exciting possibilities for future developments on large-scale compact integrated switch design on the IMOS platform.

Acknowledgments

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References

[1] L. Poutievski *et al.*, “Jupiter evolving: Transforming googles datacenter network via optical circuit switches and software-defined networking,” in *SIGCOMM 2022 - Proceedings of the ACM SIGCOMM 2022 Conference*, Association for Computing Machinery, Inc, Aug. 2022, pp. 66–85. doi: 10.1145/3544216.3544265.

[2] N. P. Jouppi *et al.*, “TPU v4: An Optically Reconfigurable Supercomputer for Machine Learning with

Hardware Support for Embeddings," in *Proceedings - International Symposium on Computer Architecture*, Institute of Electrical and Electronics Engineers Inc., Jun. 2023, pp. 1147–1160. doi: 10.1145/3579371.3589350.

[3] Y. Wang, S. Bhat, B. Shi, T. Aalto, and N. Calabretta, "C- and L-band low polarization sensitive nanosecond 1×2 electro-optic MZI switch on 3-μm thick silicon platform," p. M4J.3, May 2023, doi: 10.1364/OFC.2023.M4J.3.

[4] D. W. Feyisa, B. Shi, R. Kraemer, N. Calabretta, and R. Stabile, "Compact 8×8 SOA-Based Optical WDM Space Switch in Generic InP Technology," *Journal of Lightwave Technology*, vol. 40, no. 19, pp. 6331–6338, 2022, doi: 10.1109/JLT.2022.3197292.

[5] K. ławniczuk, L. M. Augustin, N. Grote, M. J. Wale, M. K. Smit, and K. A. Williams, "Open access to technology platforms for InP-based photonic integrated circuits," *Advanced Optical Technologies*, vol. 4, no. 2. Walter de Gruyter GmbH, pp. 157–165, Apr. 01, 2015. doi: 10.1515/aot-2015-0012.

[6] D. W. Feyisa, S. Abdi, R. van Veldhoven, N. Calabretta, Y. Jiao, and R. Stabile, "Low Polarization Sensitive O-band SOA on InP Membrane for Advanced Photonic Integration," *Journal of Lightwave Technology*, 2024, doi: 10.1109/JLT.2024.3369232.

[7] S. Abdi *et al.*, "Research Toward Wafer-Scale 3D Integration of InP Membrane Photonics With InP Electronics," *IEEE Transactions on Semiconductor Manufacturing*, 2024, doi: 10.1109/TSM.2024.3382511.

[8] Y. Jiao *et al.*, "InP membrane integrated photonics research," *Semicond Sci Technol*, vol. 36, no. 1, 2020, doi: 10.1088/1361-6641/abcadd.

[9] "Mathematical theory of connecting networks and telephone traffic / V.E. Benes - Catalogue | National Library of Australia." Accessed: Apr. 26, 2024. [Online]. Available: https://catalogue.nla.gov.au/catalog/2448178

[10] H. R. Mojaver *et al.*, "8 × 8 SOA-based optical switch with zero fiber-to-fiber insertion loss," *Opt Lett*, vol. 45, no. 16, p. 4650, 2020, doi: 10.1364/ol.399415.