Research towards wafer-scale 3D integration of InP membrane photonics with InP electronics

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***Abstract*—In this study, we focus on the development of key processes towards wafer-scale 3-dimentional/vertical (3D) integration of Indium-Phosphide (InP) photonic membranes on InP electronics via adhesive bonding. First, we identified the most critical steps and optimized them to achieve high thermal and mechanical compatibility of components for the co-integration process. Next, we developed a strategy for InP-to-InP wafer bonding with high topology tolerance, and introduced hard Benzocyclobutene (BCB) anchors to preserve the alignment and BCB thickness uniformity after bonding. The resulting bond layer is homogeneous in terms of physical and mechanical properties. Finally, we developed a novel method to selectively remove the InP substrate from the photonics side via wet etching while protecting the electronics carrier wafer with hermetic multi-layer coatings. The investigation of these key steps for is essential for scalable 3D integration of photonics and electronics at ultra short distances.**

***Index Terms*—3D integration, adhesive bonding, co-integration, InP electronics, membrane photonics**

I. Introduction

The prolific use of the Internet and the high performance computing needs for artificial intelligence (AI) models are driving the exponential growth of datacenter traffic [1], [2]. This increases requirements for versatile higher speed data communication beyond 800 Gb/s and at energy consumption below 5pJ/bit [3]. However, current transceiver technologies are limited in terms of bandwidth scaling and energy efficiency, with bottlenecks not only restricted to the electrical/optical (E/O) devices, but also to the connections in-between [4]. For current pluggable transceivers, the driving electronic integrated circuits (EICs) and light-emitting photonics integrated circuits (PICs) are mounted side-by-side on a printed circuit board PCB, and hybrid interconnections are realized through wire bonds. This limits the system's bandwidth due to the RF parasitic losses of long wires and poses significant costs to packaging [4]. This assembly also requires high footprints, which is limited and increasingly more constrained for pluggable modules. On systems' level, the industry is shifting towards Co-Packaged Optics (CPO) where the optics are placed in the same package as the host integrated circuit for more compactness, bandwidth, and energy efficiency, which is not supported by the aforementioned wire bonding approach [2], [5], [6]. Closer integration of EICs with PICs is becoming increasingly important for the development of both pluggable and co-packaged optics. Numerous EIC-PIC integration schemes where the two are closely connected with no wire bonds have been demonstrated, with short interconnects being key to preserving the E/O bandwidth and power consumption of these devices at a systems' level [5], [6]. A 2.5D approach demonstrated energy consumption as low as 170 fJ/bit at 25 Gb/s [2], [5], [6]. Ultimately, 3D integration of PICs on top of EICs offers the most optimal way to narrow the physical distance between the two. It significantly reduces RF parasitics [7], and achieves a higher interconnect density toward new systems on chip with higher complexity and lower cost [4], [8], [9].

This 3D integration is very promising, especially since ultra-high-performance devices with high downscaling potential can be intimately integrated [10]. Moreover, InP is prized for its exceptional electronic and optoelectronic properties. For instance for electronics, InP electronics offers ultrahigh-speed transistor technologies with beyond 1 THz frequency cutoff, such as high electron mobility transistors (HEMTs) [11] and double heterojunction bipolar transistor (DHBT) [12], [13]. Moreover, unmatched driving circuit bandwidths beyond 200 Gb/s were demonstrated based on those devices [13], [14]. For photonics, InP photonics transmitter and receiver components with performance beyond 100 GHz and toward THz regime were achieved, as these devices are not limited by the physical properties of InP at these bandwidths [15]. For example over 300 GHz single InP-based photodetector modules were recently demonstrated [16]. Intimate co-integration of the electronics and photonics layers can be realized with wafer-scale bonding, followed by lithographically defined

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interconnects, to offer the highest scalability in terms of fabrication and packaging cost and yield.

This paper is organized as follows. In section II we introduce the co-integration scheme discussed in this paper from the perspective of electronic/photonic devices and optical/electrical connections in-between. In section III we discuss the fabrication flow and identify its related major challenges. In section IV we investigate these challenges, and finally we conclude our work in section V.

II. Co-integration scheme

Fig.1.a shows the electrical and optical wiring scheme of the receiver and transmitter sides of a transceiver, Fig.1.b shows a false-scale schematic cross-section of the vertical stack with InP membrane photonic devices on top of InP DHBTs co-integrated in the wafer-scale. We refer to the photonics as membrane devices as these are fabricated on a micrometer-thick epitaxial layer suspended on a low index material, which allows for achieving photonic devices with nanoscale dimensions [17]. These are bonded with BCB to the electronics. The E/O devices are connected with ultra-short (<15µm) and lithographically defined through-polymer gold (Au) vias (TPV). TPVs allow for very low RF and DC losses for maintained signal integrity, and higher spatial scalability compared to bond wires and flip-chip bumps that are currently commonly used for packaging interconnects in 2D and 2.5D schemes, at the chip scale [6], [7], [18]. Moreover, the TPVs are lithographically defined at wafer scale [9], allowing for high density interconnects and high assembly scalability in terms of chips per wafer and costs per chip, for given EIC and PIC technologies.

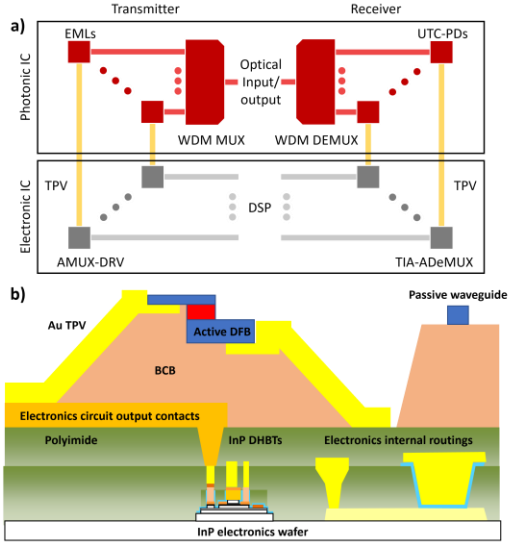

Fig. 1. a) Electrical and optical scheme of the co-integrated transmitter and receiver, b) schematic illustration of the co-integrated InP photonics and electronics, dimensions are not to scale

For this scheme, the optical signal is transmitted laterally between inputs/outputs and photonic components through passive waveguides (light red in Fig.1.a). The electrical signal is transmitted vertically between the photonics and electronics with (TPV) (golden yellow in Fig.1.a) [9]. At the transmitter, an externally-modulated laser (EML) generates and modulates the optical carrier. Simultaneously, the electrical signals from the digital signal processing unit (DSP) are multiplexed to increase the link throughput with an analog multiplexer (AMUX), [7], [14]. The last monolithically integrates a linear modulator driver (AMUX-driver) to ensure a sufficient extinction of the optical carrier at the transmitter output. Modulated optical signals from multiple transmitters are aggregated through wavelength division multiplexing (WDM). At the receiver, the optical signal is collected and demultiplexed using WDM into separated wavelengths. The latter are detected in multiple high-speed photodiodes. Each are converted into an electrical signal that is transmitted vertically through TPVs to the transimpedance amplifier (TIA)-analog demultiplexer (ADeMUX) to be subsequently re-amplified and demultiplexed before passing through the receiver DSP [8].

III. Fabrication flow and challenges

Asides from the careful co-design of the InP photonic and electronic components taking into account thermal, electrical and optical boundary conditions, several technological challenges need to be overcome for successful co-integration. In this section, we briefly present an overview of the fabrication flow and associated challenges with the multiple steps, focusing mostly on those covered by this paper. Fig.2 shows a schematic illustration of the major steps related to this flow. For this scheme, we integrate InP DHBTs that are fully fabricated and functional to semi-fabricated InP membrane photonics via adhesive bonding with BCB. This represents a major advantage as the fabrication flow for the photonics and electronics remains similar to the original process with no compromises to each other. The state of these wafers before integration is simplified as shown Fig.2.a, with photonics and electronics having topologies of approximately 2µm and 6µm, respectively. All of these fabrication steps are realized on the wafer scale using 3-inch substrates and support scalability to larger substrates.

The integration process starts with preparing the semi-fabricated photonics wafer and the fully fabricated electronics wafer for bonding (Fig.2.a). This involves the deposition and outgassing of 500nm SiO_2 that promotes adhesion of BCB to the substrates. Next, we spin-coat and soft-bake 10- to 12-µm of BCB on the electronics side, targeting a thickness that is close to double the topology on the wafer for better planarization (Fig.2.b). As for the photonics wafer, we deposit the SiO_2 layer and follow it with the fabrication of SiN backside markers. Afterwards, we fabricate the hard BCB anchors, which we pattern by photolithography and dry etching (Fig.2.b). We target the same BCB thickness (10- to 12-µm) so that the anchors reach the other substrate. The functionality of anchors is discussed later in this section. The two wafers are then aligned with the wafer backside alignment method [19], i.e., with font-side markers from the electronics wafer and back-side markers from the photonics wafers, and subsequently bonded in controlled temperature environment (Fig.2.c). Here, BCB crosslinks to permanently join the two wafers with a high bond strength and low electrical, electromagnetic, and thermal crosstalk between the two interfaces (Fig.2.c). A post-bond uniform interface is achieved as both anchors and bond layer are fully baked. Next, we remove the SiN backside markers, clean the bonded stack from residual BCB, and deposit protective coatings on the backside of the electronics wafer, i.e., the substrate to be preserved (Fig.2.d). The latter is realized as

the photonics substrate is removed via selective wet etching with an etch-stop layer (Fig.2.e), i.e., the photonics layers in combination with the backside coatings protects the electronics carrier wafer from damage. Subsequently, the post-bond fabrication of photonics is continued as part of the double-side processing, i.e., their processing take place before and after bonding for better design freedom [17]. Finally, BCB is opened in areas near contacts and the E/O devices are connected with ultra-short (<15µm) TPV (Fig.2.f). This is realized with photolithography and electroplating of Au to reach a thickness of approximately 5µm followed by Au seed layer removal with wet etching.

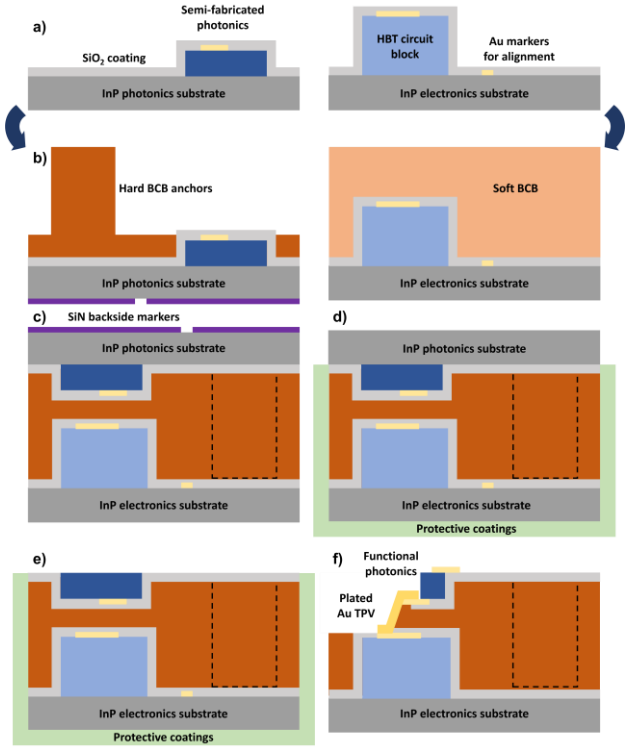

Fig. 2. Major integration process steps, a) before integration, b) wafers prepared for bonding, c) after bonding, d) deposition of protective coatings, e) photonics substrate removal, f) continued fabrication of photonics, then TPV

Bonding and post-bonding processes are inherent to membrane photonics fabrication, so they do not affect their performance nor add additional fabrication steps [17]. However, these processes were not tested on functional electronics. The performance of DHBTs can be affected by the thermal treatments and mechanical stresses introduced during the bonding process. Bonding is realized at a temperature above 200°C for several hours [19], while other post-bonding steps can be at higher temperatures. Hence, an accurate assessment of the thermal tolerance of the DHBTs is required to determine their compatibility with this integration scheme and to define process boundary conditions that respect these limitations. The performance of the DHBTs at various thermal conditions. i.e., time, temperature, and ramp-up rate, was studied and is presented in section IV.A. Moreover, InP DHBTs are embedded in SiO_2 and BCB after integration (Fig.2.c-f). Temperature ramping during bonding causes BCB to expand at an order of magnitude higher than InP, which can result in residual stress build-up that affects the InP DHBTs, or BCB delamination during DHBTs contact open. Thus, a process with low-stress SiO_2 needed to be developed, and assessment of DHBTs performance after opening contacts was conducted. A study on this is presented in section IV.B. The stress of BCB was also assessed for various thicknesses and results are presented in section IV.D.

After the bonding process, the InP photonics substrate needs to be completely removed to leave only the micrometer-thick epitaxial layer. This is realized with wet etching using concentrated Hydrochloric (HCl) acid over an extended duration [17]. However, since both of the photonics and electronics wafers are InP-based, the electronics carrier wafer has no chemical selectivity to the solution. Hence, it needs to be preserved with hermetic coatings that covers its backside and edges. InP is very fragile and brittle compared to other substrates such as Si or Glass, so defects introduced from HCl attacking open spots and leakage paths can be detrimental to post-bonding processing. The development of low-stress multi-layer protective coatings is discussed in section IV.C.

Preserving the wafer-to-wafer alignment during bonding is crucial to connect the photonics with electronics. Bonding with soft-baked BCB ensures a void-free bond with high bond strength [19]. However, the soft BCB reflows during bonding and causes the two substrates to misalign in orders of tens to hundreds of micro-meter before turning solid again, which can lead to degradation of the via performance or even failure of the integration process [4]. In our earlier works we developed a process with hard BCB anchors that provide solid support during this phase and prevents misalignment, which was tested on transparent glass-to-glass bonding with no topology [20], [21]. Misalignment values were suppressed from 50-100um to below 10µm. In this work, we first developed backside markers to allow for InP-to-InP back-side alignment bonding, and also investigated the effectiveness of BCB anchors for InP-InP bonding with/without topology, which has not been investigated before. Results are presented in section IV.D. Here, the experimental conditions were set respecting the findings from the study of temperature budget (section IV.A) and the selective substrate removal (IV.C).

Also, bonding with soft BCB results in high post-bond BCB thickness non-uniformity on the wafer scale [21]. This arises from non-uniformities in the local pressure applied to the wafer during bonding. Using BCB anchors reduces significantly this non-uniformity, which is also treated in the same section. Moreover, as discussed before, the residual stress of BCB for different BCB thicknesses and treatment times was also investigated. This is because the hard anchors further densify during the bonding process, so high residual stress mismatch between anchors results in non-uniform mechanical properties across the bond layer, which can compromise the durability of the stack. This was investigated and presented in the same section.

For electrical connections, low parasitic resistance, and break-free TPV were designed and fabricated on Si substrate with BCB thicknesses in the 7-20µm range [18], [22]. These demonstrated an RF 3 dB bandwidth beyond 67 GHz, and this value was only limited by the measurement equipment [18], [22]. Similar structures are adopted for this co-integration scheme to guarantee similar performance but with a thicker (5µm) TPV for heat sinking as discussed next.

For thermal management of the 3D stack, active thermal management is applied from the electronics side. This is more effective than active cooling from the photonics side only as the electronics typically consume more electrical power and generate more heat, hence dissipating their heat is more difficult [23]. Cooling is realized by placing a thermoelectric cooler on the bottom of the InP DHBTs substrate after thinning it to 150µm. However, managing the heat generated by photonics is required. The heat, in this scenario, will be conducted from the hotpots in the photonics layer to the heat sink through the bonding layer and the electronics structures. Here, the thick TPV used for electrical interconnects also acts as a heat sink for photonic devices, which has previously demonstrated [24], [25].

Finally, the micrometer-thick membrane is prone to spatial distortions resulting from the bonding process, which can degrade the overlay accuracy in post-bonding lithography steps. However, these distortions were found to be minimal in the case of bonding InP on InP because of the identical physical properties, and hence are not concerning [26].

IV. VALIDATION OF MAJOR STEPS

A. Thermal compatibility of III-V electronics with the integration process

Here, we systematically studied the effects of thermal treatments on InP electronics. For this purpose, high-speed > 350-GHz transition frequency (f_T) DHBTs with 0.7µm emitter width were fabricated at III-V Lab [27] on a 3-inch InP epitaxial wafer. After wafer thinning and dicing into small samples containing multiple DHBTs as shown in inset of Fig.3.b, thermal treatments were carried out on individual samples. The process parameters for integrating, functionalizing, and connecting photonics with DHBTs described earlier requires various thermal treatments. These include the bonding, the deposition of oxides and nitrides, the dry etching of BCB and semiconductor, and the metallization for TPV. The temperature for most of these processes can be tailored in the range of 80-300°C if required. Hence, values as high as 300°C for short durations need to investigated to define a safe process flow for DHBTs. This is because the DHBTs fabrication window does not exceed ~250°C [27]. We note that adhesive bonding thermal budget is (time × temperature) is the highest among other processes. The temperature budget tests were realized in EVG520 bonder at vacuum level (<10^{-5} Torr) to mimic the same environment and temperature cure as in real bonding, but results extend to other processes as well. The studied temperature range is 200-300 °C, with ramp rates of 2, 5, and 10 °C/min, respectively. A large range of treatments time was investigated with values of 0.5, 1, 2, 5, 10, and 20 hours. Compiling these 3 parameters yielded 24 distinct process variations, which fully cover all the post-bonding process parameter space.

The DC and RF performance of the InP DHBTs was measured on-wafer before the thermal treatments and on thinned samples after the thermal treatments. Some DHBTs were also measured on a thinned sample before treatments for comparison. Their DC performance was assessed using $I_C(V_{CE})$ curves and transition frequency f_T was extracted from S-parameter measurements, results are shown in Fig.3. Their post-treatment integrity was determined based on the degree of degradation in their functionality, for example by a variation in their emitter series resistance (R_E) and f_T.

Firstly, it should be noted that the extracted f_T on thinned sample are ≈5% lower than those on on-wafer, which is due to a small increase of the base-collector transit time likely resulting from additional self-heating effects after wafer thinning. This is taken into account when assessing thermally treated samples. As a result of the treatments, DHBTs treated at 240 °C (and below) showed identical DC and RF characteristics compared with their pre-treatment performance, regardless of treatment times between 10-20 h and ramp rate between 5-10°C/min, as shown in Fig.3.a) and 3.b). Treatment temperatures of 260°C resulted in a slight degradation of R_E and f_T for treatment times above 1h. However, samples baked at 280°C strongly degraded, with a 62% increase in R_E, and subsequent decrease of f_T for treatment time of 2h, as shown in Fig.3.c) and 3.d). Devices baked at 300 °C showed significantly degraded f_T, which dropped below 350 GHz, even at treatment times of only 0.5h. Additionally, we observed no noticeable effect of the ramping rates in our experiments.

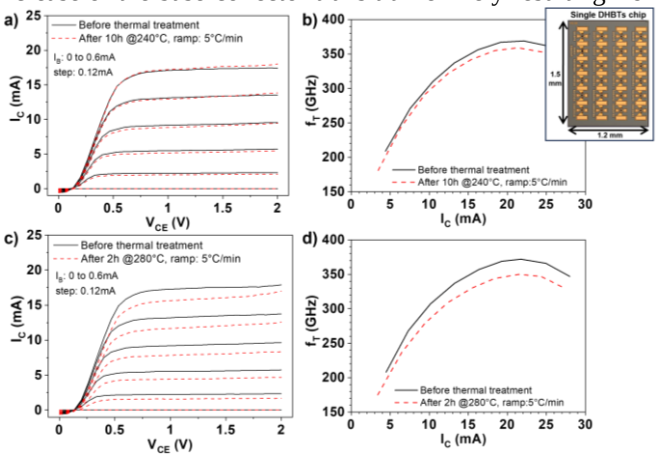

Fig.3. a),c) DC, b),d) f_T curves of 0.7x5µm² InP DHBTs before and after baking at temperature, time, and ramp speed of: a) and b) 240°C, 10h, and 5°C/min, c) and d) 280°C, 2 h, and 5°C/min. Top Inset: InP DHBT sample.

Both outgassing of the SiO_2 layer used for bonding and the bonding process itself are usually carried out at 280°C for 1h [19]. This is to ensure void-free bonding and 100% crosslinking in BCB. Identical results can be achieved with lower temperature of 240°C and longer treatment of 10h as BCB crosslinking requires more time for lower temperatures [19]. However, we found that a combination of 2h at 240°C is sufficient for oxide outgassing since we shifted from PECVD to inductively coupled plasma chemical vapor deposition (ICP-CVD) SiO_2 (see details of the process in section IV.B), which contains less trapped gasses. For bonding, 9h at 240°C is sufficient for >97% BCB crosslinking. Hence, these parameters were chosen for co-integration. A bonding test with these parameters and optimized protective coatings (see section IV.C) was carried out, and void-free bonding was demonstrated.

B. Effect of SiO_2 and BCB residual stress on InP electronics performance

As mentioned, the DHBTs are embedded in BCB and SiO_2 after the co-integration process. To examine the impact of these additional dielectrics applied on the devices, we tested the performance of 0.7µm InP DHBTs under the presence of residual stress from SiO_2 and BCB. We used two InP cleaved samples containing multiple DHBTs for this purpose. Sample 1 was used to study the stress induced by 500 nm SiO_2 layer, which is required as part of the protecting coatings (see section IV.C). The ICP-CVD SiO_2 layer has a residual stress <100 MPa, measured by the wafer bow method using profilometry. Sample 2 was used to study the combined stress from 500nm SiO_2 and 12µm BCB deposition, mimicking the stack in the real process. The residual stress of BCB is below 50MPa (see section IV.D). Both SiO_2 outgassing and BCB full cure were performed at 240°C for 10h. To access the contacts and measure DHBTs, contact openings were then defined with photolithography and dry etching in CHF_3 plasma. Cross-section schematics of sample 1 and 2 are shown in Fig.4.a and Fig.4.b, respectively. Here, only the probing pad areas are opened, whereas the HBT core is still covered in these layers. Etching of SiO_2 and BCB was done using the same O_2:CHF_3 20:4 chemistry where etching times of 40 min and 3h30 min were required to clear the layer and reach contacts in sample 1 and 2, respectively.

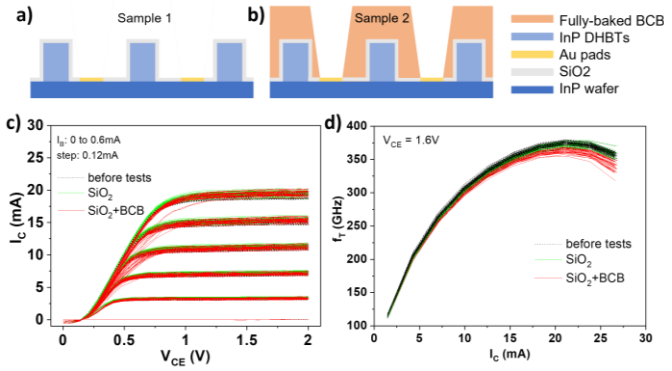

Fig.4. Schematic representation of the stacks dedicated for stress tests of: a) SiO_2, b) SiO_2+BCB. Electrical response of 0.7x5 µm² InP DHBTs before and after adding SiO_2 and SiO_2 +BCB: c) $I_C(V_{CE})$ characteristics, d) f_T vs collector current at V_{CE}=1.6V

The number of characterized transistors is 80 before the processing, 26 after SiO_2-only deposition, and 36 after SiO_2+BCB deposition. Superimposed $I_C(V_{CE})$ and $f_T(I_C)$ at V_{CE}=1.6V curves are shown in Fig.4.c and 4.d, respectively. As shown in Fig.4.c), the saturation slopes for sample 1 match the ones before processing and the transistors were not affected by the SiO_2 layer. Measurements performed on sample 2 showed a slight degradation on $I_C(V_{CE})$ saturation slope, which is linked to an average 20% increase in R_E compared to measurements before processing. The same degradation is observed for the 0.5-µm emitter width devices. From Fig.4.d, it can be seen that the transition frequency f_T dropped by an average of <5% for sample 2 compared to sample 1 and the data before processing, which was also linked to the increase in R_E.

Since the total treatment time and temperature of 20h at 240°C respected this budget for sample 2, the degradation is likely related to the extended time in etching required to etch BCB in the RIE plasma process where high pressure is required. Moreover, as the DHBTs performance is temperature-dependent, we carried out thermal simulations to assess the temperature of HBT circuits with/without thick BCB coatings on top. However, a difference below 1°C (≈4%) was witnessed between the two cases since most of the heat is dissipated from the substrate through heat conduction. Overall, high RF performances were demonstrated despite this slight degradation. However, as discussed earlier, the bonding process was optimized where the outgassing time was reduced to 2h and baking to 9h at 240°C to allow for a larger thermal window to other post-bonding processes.

C. Multilayer protective coatings for low-damage InP substrate removal

Substrate selective removal is a key process to reach the photonics membrane epilayer with precise thickness and without introducing microcracks or defects to the membrane and carrier wafer. In this InP-to-InP co-integration scheme, it is particularly crucial since the carrier wafer to preserve is of the same material system as the one to be removed. Selective wet etching with the assistance of an etch-stop layer is the most commonly used method [17]. Etching is done using concentrated HCl:H_2O 4:1 at 35 °C for 1h to remove 650µm of InP, which creates gaseous PH_3 by-products. For InP-InP bonded wafers, this requires conformal and hermetic backside protection to block the solution from damaging the electronics carrier wafer. InP is very fragile, so areas attacked by the acid become week points that can compromise further processing [28]. Thus, low-stress conformal and hermetic coatings are needed. Additionally, the deposition and removal of these protective coatings need to be within the thermal processing window discussed in section IV.A.

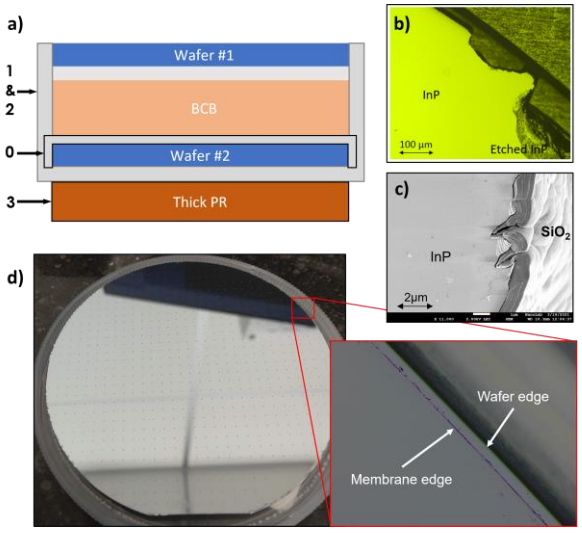

Fig.5. a) schematic illustration of the layer stack. L:0-3 indicates the deposition order of these layers, b) SEM image of InP wafer edge covered with 1µm SiO2, c) Image from the wafer edge of experiment N#1, d) image of an InP membrane on InP wafer after substrate removal

Having these considerations in mind, we systematically investigated different combinations of protective layers. A schematic illustration of the tested coatings where wafer #2 is protected is shown in Fig.5.a. Table.1 shows the experiments realized within this frame. Wafer #1 in these experiments is a

bare InP substrate with no epilayers, so it is totally removed after the wet etching. This makes it easier to inspect the bonding interface and wafer #2 after the wet chemical steps. Also, layer 0 is the SiO_2 layer used to promote the adhesion of BCB to the substrate, layers 1 and 2 are composed of SiO_2 deposited after bonding to cover the backside and edges. Layer 3 is a spin-coated resist layer that covers the backside for full hermicity. It should be noted that after the bonding process, we always first clean the backside in O_2:CHF_3 20:4 plasma to remove any residue of BCB before depositing layers 1-3.

TABLE I
EXPERIMENTAL TESTS REALIZED TO INVESTIGATE PROTECTIVE COATINGS

Exp N	Adhesion SiO_2 (50 nm)	Adhesion SiO_2 (500 nm)	Thin ALD SiO_2 (<100 nm)	Thick CVD SiO_2 (>1µm)	Thick resist (30 µm)
1	0	/	/	/	3
2	/	0	/	/	3
3	0	/	/	2	3
4	/	0	/	2	3
5	/	0	1	2	/
6	/	0	1	2	3

We first investigated the required SiO_2 (L0) thickness for good BCB adhesion to the top interface of the protected InP wafer (#2) [29]. The tested thicknesses are 50 and 500nm. This was done in the first 4 experiments with 50 nm used in experiment 1 and 3 and 500 nm in 2 and 4. For backside protection, a thick 30µm resist is deposited for experiments 1 and 2, while 3 and 4 also have 1 µm of SiO_2 before the thick resist. The SiO_2 is deposited in ICP-CVD at 80°C and the resist is baked at 110°C. The findings revealed that using 50nm thickness for L0 resulted in BCB delamination near edges during the wet etching, which damaged the underlying InP in exposed spots. Edge defects larger than 100µm were found in experiment 1 (Fig.5.b). Using thicker adhesion SiO_2 (L0) resulted in much smaller defects both for experiment 2 and 4 compared with 1 and 3, with experiment 4 having the lowest density of defects. We note that the density here was only qualitatively assessed by optical microscopy. Moreover, the defects are larger in size in experiments 1 and 2 compared with 3 and 4. This is because the 1 µm SiO_2 covers the wafer edge to a good extent (Fig.5.c), whereas the thick resist only marginally covers it. Moreover, the backside surface of wafer#2 is fully preserved in all experiments.

However, from Fig.5.c, it can be seen that the 1µm SiO_2 cannot fully cover the micro-cracks on the wafer edge since the deposition is anisotropic. Hence, a <100nm thin SiO_2 atomic layer deposition (ALD) layer was introduced first for conformal coverage. ALD deposition is realized at 200°C. To test if the ALD SiO_2 can fully preserve the backside surface and the edge of wafer#2, we realized exp5 and 6. For exp 5, we used 500nm adhesion SiO_2 on top of wafer#2 and its backside was protected with the ALD SiO_2 followed by 1µm ICP-CVD SiO_2, while the thick resist was not used. For exp 6, we used all of the layers L0-L3. For results, the density of edge defects in both exp5 and 6 was significantly reduced owing to the conformal coverage of SiO_2, with few small defects of dimensions <10µm. However, the backside surface in exp5 contained multiple etch pits with sizes in the 50-100µm range while it remained pristine in exp 6. This is because the wafers are extensively processed up to the point of bonding, so the backside surface contains more pinholes and scratches, and is contaminated with particles that can detach during the etching process and reveal exposed areas. Hence, the presence of a 30µm thick resist layer helps in covering these particles and preserving the backside surface during etching. Both deposition and removal of these coatings are compatible with the DHBTs thermal stability. The resist can be dissolved in acetone at 25°C and SiO_2 can be dry etched at a temperature <200°C. Hence, the combination of protective coatings used in experiment 6 is suitable for the co-integration. To validate this, we tested the combination again, but with wafer #1 having a ≈1µm epitaxial layer stack. An image of the wafer after substrate removal is shown in Fig.5.d. Here, the edge of the wafer is well protected with no visible etch defects.

D. Preserving the alignment accuracy and BCB thickness uniformity using Anchors

To investigate the effect of BCB anchors on post-bonding properties, we realized three InP-InP bonding experiments with backside alignment, as described in section III. The first is a reference bond with no anchors, labeled as sample 1, whereas the second (sample 2) and third (sample 3) experiments do contain anchors. The difference between sample 2 and 3 is whether they contain surface topology or not. Table II summarizes these details. A schematic illustration of the InP-InP alignment bonding for sample 3 is shown in Fig.6. Wafer #1 and #2 represent the electronic and photonic wafers, respectively. The targeted BCB thickness is 10 µm as discussed in section III. For sample 2, wafer #1 has no topology except for the Ti/Au markers with a thickness of about 100 nm. As for sample #3, wafer #1 contains 3 µm of topology, similar to the actual electronics wafer. In all experiment, preparation of wafer #1 for bonding consists of depositing and outgassing 500 nm of SiO_2 (see section IV.C) for 2h at 240°C, followed by spin coating of 10 µm of BCB (Cyclotene 3022-63) and soft baking. As for wafer #2, we first fabricated Ti/Au front-side markers with lift-off. Next, we fabricated backside markers on wafer #2 (Fig.6.a), aligned to the Ti/Au front-side markers. The backside markers are realized by depositing a SiN layer, then patterning it with photolithography and dry etching in CHF_3 plasma.

TABLE II
SUMMARY OF INP-INP CO-INTEGRATION ALIGNMENT BONDING TESTS

Sample N	Bond layer BCB thickness (µm)	BCB anchors height (µm)	InP topology (µm)
1	10	0	0
2	10	10	0
3	10	10	3

To fabricate BCB anchors, we first spin-coat the wafer with 10 µm of BCB (also Cyclotene 3022-63) and fully bake it. Baking is realized at 240°C for 9h in order to reach full-crosslinking (section IV.A). Anchors are then fabricated by photolithography and dry etching in CHF_3:O_2 plasma. Full details can be found in [20]. The layout of the anchors is designed based on the electronics layout where anchors of 100x100µm^2 are placed in all dice line areas and cells used for testing, covering 20% of the total 3-inch area similar to our previous study [20]. A sideview SEM image of the anchors is shown in Fig.6.c. Their 3D shape is achieved by reflowing the resist, resulting in smooth corners and a sidewall angle of 37° that improves the contact surface area between them and the

bond layer. For all experiments, the bonding was realized at 240°C for 9h at ramp rate of 5°C/min. This is different from the previous study which was done at 280°C for 1h at ramp rate of 10°C/min [20]. Here, the slower ramp-up leads to a longer process time during which the BCB may reflow. This can potentially result in a higher misalignment. After bonding, the BCB densifies, and a uniform layer is achieved (Fig.6.b).

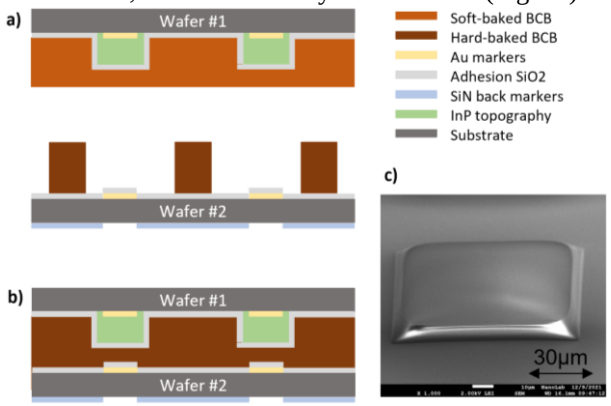

Fig.6. Schematic illustration of the bonding stack, a) before bonding, b) after bonding. c) SEM image of fabricated BCB anchors

Hard BCB anchors serve as a mechanical backbone that suppresses the lateral displacement in the (x,y) plane of the substrates [20]. Here, x and y are directions in the wafer plane with x being parallel and y perpendicular to the wafer major flat. For accurate analysis, we average the extracted misalignment from markers distributed in the wafer scale. An example of markers misaligned in sample 1 and 3 are shown in Fig.7.a and 7.b, respectively. The wafer-scale average misalignment values in the (x,y) plane in µm for experiments 1, 2, and 3 are (24.6, 5.3), (8.2, 4.2) and (7.3, 5.8), respectively. These values take into account the fundamental alignment inaccuracies from the bonder tool during backside marker fabrication and wafers alignment for bonding, which are both in the order of 1-2µm [19]. Hence, the misalignment decreases by at least 15µm to values below 10µm with the addition of anchors for this BCB thickness, i.e., >150% improvement. This is sufficient for co-integration since the pad areas are typically in the order of 50-100µm in size. Moreover, compared with sample2, the introduced topology in wafer#2 for sample3 did not affect the misalignment values, which guarantees the feasibility of this process for real co-integration. Also, these values are similar to the experiments realized by bonding glass to glass at higher ramp up rate of 10°C/min [20], which signifies that the method can be used for a wide range of materials.

For the physical properties, void-free bonding was achieved in all of these experiments. We also inspected the BCB thickness variations of these samples. A map of the thickness variation of sample 1 is shown in Fig.7.c, as an example. The variation in thickness, measured from peak to valley, is 91%, 26%, and 34% for samples 1, 2, and 3, respectively. This indicates that anchors help greatly in decreasing thickness variations across the bonded wafers, which is crucial for post-bonding processes. This variation is slightly higher for sample 3 compared with sample 2, which deserves further investigation in the future.

We also investigated the residual stress in the anchors and the bond layer to assess if the bonding interface is uniform in terms of mechanical properties. This is also relevant for section IV.B as the amount of stress from BCB is investigated. A stress mismatch can result for instance from higher densification of BCB after full cure [30], since the BCB anchors are fully cured and then further treated during bonding. This is especially important if the anchors are close or embedding devices, for instance if the layout does not offer free space for anchors. BCB stress for different baking temperatures was previously studied [31]. However, BCB stress for different thicknesses and treatment time are needed in view of the co-integration. Thus, we concentrated on these two parameters. For this, BCB is

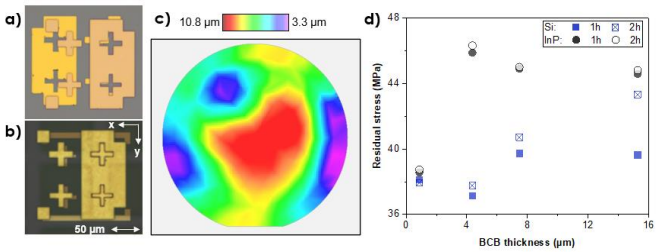

Fig.7. Post-bonding alignment markers for InP-on-InP: a) without anchors, b) with anchors. c) post-bonding thickness uniformity without anchors on the 3-inch wafer. d) Residual stress of BCB deposited on InP and Si and treated at 280 °C for 1h and 2h.

deposited in the thickness range of 1-16 µm on top of InP and Si substrates for comparison. We treated the samples at 280°C for 1h, corresponding to the post-bonding bond layer BCB crosslinking state, and 280°C for 2h corresponding to the anchors' BCB crosslinking state. These are similar thermal budget to the earlier experiments and are only used to accelerate the process. The wafer bow was measured in multiple directions across the wafer using profilometry, and the stress is assessed from the variation in bow before and after the treatment using Stoney's formula [32]. For comparison, we also calculated the theoretical maximum residual stress that results from CTE mismatch between BCB and the substrates [31]. The corresponding BCB thicknesses to the treatments of 1h and 2h were tracked with reflectometry for better accuracy.

Fig.7.d shows the residual stress of BCB deposited on InP and Si and treated at 280 °C for 1h and 2h. The theoretical BCB residual stress treated at 280°C is 67.5 MPa for BCB on Si and 65.2 MPa for BCB on InP. However, the experimental values are between 36-48 MPa for all BCB thicknesses. This results from the partial relaxation of BCB stresses given the mobility of polymer chains at this temperature [31]. More importantly, all stress mismatch values between BCB treated for 1h and 2h are below 5MPa for both BCB on Si and on InP. This difference is low because BCB stress is mainly dominated by the treatment temperature. Finally, these results confirm that a bonding interface where BCB anchors are present is uniform in terms of residual stresses for multiple substrates including InP.

V. Conclusion

In this paper we presented a novel fabrication scheme for 3D integration of InP membrane photonics on InP electronics on the wafer scale. We focused on investigating and improving all crucial steps to enable this scheme. This includes studying the thermal and mechanical compatibility of active components with integration processes, development of protective coatings for defect-free substrate removal, and the introduction of BCB anchors to preserve the alignment and BCB thickness uniformity after bonding. We also show that the bonding

interface is uniform in terms of physical and mechanical properties.

This cohesive fabrication scheme will enable photonic devices integrated on electronics with ultra-short interconnections for high-speed and low-power operation. The approach also transfers some of the packaging steps from the die scale to the wafer scale, which could lower the cost and improve the performance for chip assemblies.

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