Ultra-Compact 8×8 Optical Space Switch with Generic InP Technology

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ABSTRACT
A broadband and fast optical space switch is a crucial part of optical networks. A broadband, compact, and fast monolithically integrated InP/InGaAsP strictly nonblocking optical space switch based on semiconductor optical amplifiers (SOA) gates has been designed, fabricated via the generic InP technology and characterized. The component losses, gain, and switching properties of the optical switch are analysed. The gain of three SOAs on a path was measured to be 31 dB on average and is enough to balance component losses whenever a reasonable number of waveguide crossings is encountered (< 25). An optical signal to noise ratio (OSNR) and extinction ratio (ER) as large as 42.4 dB and 37.6 dB, respectively, are obtained in the best path. The performance can be further improved with optimized optical routing and design of lower loss crossings.

These results pave the way to scale the switch to higher port counts by using this switch as a building block on a modular basis. Additionally, the use of ultra-compact bends and the number of components integrated on this single chip also shows to be promising for achieving compact optical switches in generic technology.
Keywords: optical space switch, photonic integration, semiconductor optical amplifier.

1. INTRODUCTION

The persistent exponential growth of global internet protocol (IP) traffic has been continuing for decades and expected to sustain it over the coming years. Cisco forecasts the global IP traffic to almost triple from 2017 to 2022, reaching 396 Exabytes per month by 2022[1]. The implication is indeed an increase in traffic volume in core networks and, more importantly, traffic connecting to data centers, within and between data centres [2]. Not only the traffic volume, but the traffic behavior has also been changing dictated by the burst nature of the traffic demanding dynamic network reconfiguration. All optical networks are a viable solution to meet the fast speed, high capacity, and low power consumption requirement of the contemporary data centre network [3]. Therefore, optical switches are an essential part of next-generation communication, especially in data centres.

Several variants of optical switches have been explored. Switches based on MEMS have low insertion loss, low power consumption, and can scale to large port counts [4]. Silicon has an excellent thermal coefficient, which helps to tune the phase easily with low energy. However, the limited switching speed of TO and MEMS to order of microseconds and milliseconds respectively restricts their application to the static and slow portion of a network. Monolithically integrated silicon micro-ring optical switch in broadcast-select architecture has been recently reported [5]. The switch has switching extinction as high as 52 dB and crosstalk lower than -54.4 dB; however, the microsecond scale response speed and the single wavelength operation limit their use to more static traffic networks. Current highly dynamic traffic asks for broadband and fast optical switches [6].

Electro-optically actuated switches are attractive due to their fast response speed in the order of nanoseconds. Electro-optically actuated 4×4 InP cross-point switch circuit based on resonant elements was demonstrated [7], but the switching extinction is limited to less than 15dB. MZI switches based on $LiNBO_3$ also have a response speed of few nanoseconds; however, their circuit size limits their scalability [8].

SOA based circuits offer gating and amplification at the same time, have high bandwidth, and are suitable for compact and large-scale integration [9]. An active-passive broadcast and select, 16×16 rearrangeable nonblocking switch was shown in [10]. However, the inherent loss in the broadcast and select, ASE noise build-up from SOA, and injection current needed to operate it hinders the scalability. A hybrid MZI-SOA switch seems to be a viable solution to reduce losses and power consumption [11]. Viability of a 16×16 port count switch was studied by cascading two 4×4 switches, and the result showed an IPDR of 15 dB for a power penalty of 1 dB [12], however resulting in a larger footprint.

In this paper, we present an ultra-compact 8×8 port count strictly nonblocking SOA based optical switch fabricated via a generic technology and occupying only two generic cells. Ultra-steep bends, and closer SOAs are used to allow for this small footprint. In the following sections, we describe the photonic integrated circuit in section 2, followed by a discussion of the experimental procedures and results obtained in section 3. Finally, we draw a conclusion based on the experiment results obtained.

2. CIRCUIT INTEGRATION AND STRUCTURE

The designed circuit has SOA and passive sections grown within an active-passive integration scheme on InP substrate and has been fabricated by SMART Photonics foundry [13]. The active region of the SOAs are 450 μm long, include InGaASP/InP MQW optimized for TE polarization. A slightly wider active area of 3 μm compared

to the usual one is chosen to increase the output saturation power and enable WDM input operation. waveguide bends and multimode interference (MMI) splitters/combiners are deep etched. This improves field confinement, ultimately reducing device size. The mode profile in 3 µm SOA is slowly adapted to the straight waveguide through adiabatic tapers. Each SOA gate has an electrical contact pad, which is wire bonded to PCBs through which the SOAs are biased.

The switch, as shown in Fig. 1(a), has eight inputs and eight outputs, all at the same side, which are interconnected by 64 optical paths. Each port is followed by one 1:8 broadcast/combiner stage, which is implemented with seven 1:2 MMI splitters/combiners, as shown in Fig. 1(c). There are a total of 6 MMI splitters/combiners per path. The total number of SOAs on the chip is 80:16 SOAs are connected to inputs and outputs, to work as booster and pre-amplifiers, respectively, and 64 SOAs are each connected to one of the 64 routes to work as gates and amplifiers.

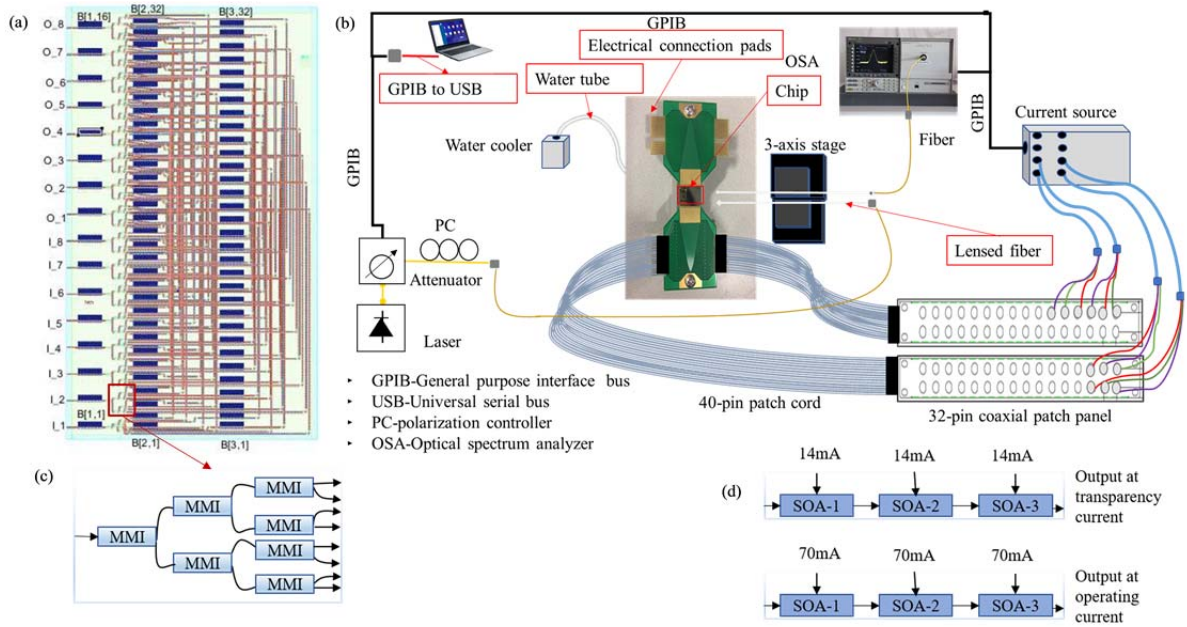

Figure 1: (a) Optical switch layout; (b) Experimental set-up; (c) 1:8 splitter; (d) Gain measurement procedure.

3. EXPERIMENTAL SET-UP AND RESULTS

A testbed has been set-up as shown in Fig. 1(b) for experimental assessment of the switch. The switch is mounted on a water-cooled heat sink and operated at 18 °C to stabilize the chip temperature. The alignment was performed via two three-axis stages with two lensed fibers used to couple the light from the laser to the chip or from it to the optical spectrum analyser. A polarization controller has been connected to the lensed fiber at the input to tune the polarization. PCB connection pad, which is wire bonded to SOAs on one end, is connected to a multichannel current controller on another end through a patch cord and patch panel. The current source supplies desired bias current to SOA gates. The current controller, the optical spectrum analyzer, and the attenuator were connected to a computer through a general-purpose interface bus (GPIB) to set the devices automatically and for automatic data acquisition. All tests were performed using a continuous wave laser input at a wavelength of 1549 nm with 0 dBm peak power.

SOA gain has been measured. The first step to determine end to end gain is to know the operating and transparency currents, and for the designed SOAs, these currents are calculated to be about 14 mA and 70 mA, respectively [14]. The on-state operating gain of three SOAs in a path was obtained by launching an optical signal to the chip and finding the difference of the signal levels at the output when the SOAs are biased at operating current and transparency current, as in Fig. 1(d). The coupling loss and path loss remain the same for both conditions, and the only thing that causes the signal level variation is the path gain. The measured average gain for representative paths is 31 dB when the SOAs are set at 70mA. A plot of gain versus input power is given in Fig. 2(c) for SOA-1 of path 6to3. It is obtained by comparing the signal level at the output when the SOA at the input is biased at operating and transparency current, keeping the other two at operating current. At the same time, the input power is varied from 7 dBm to -17 dBm at the step of 1dBm. The output saturation power for the SOA is 8dBm.

Fiber to fiber signal losses has been measured by comparing the signal levels in the input and output signal spectrum. Loss of a path depends on overall gain provided by SOAs, the number and performance of components in the path. Therefore, the chip performance is evaluated by estimating component loss to match the

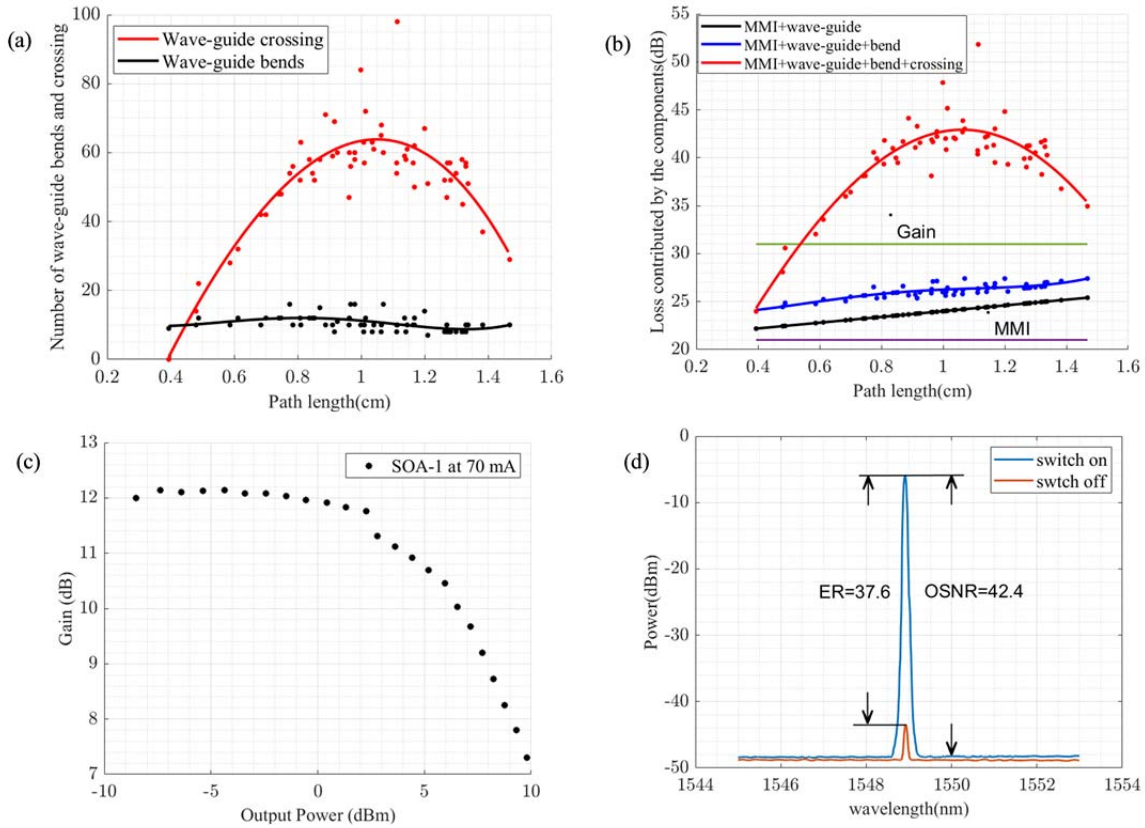

Figure 2. Plot of: (a) number of components versus path length, (b) expected on chip loss versus path length, (c) gain versus output power, (d) OSNR and ER for path 6to3.

measured and the expected fiber to fiber signal loss, which includes three quantities: the SOA gain, on-chip component losses, and the coupling loss. The on-chip component loss comes from the MMI splitters/combiners and the path-dependent loss that comes from the number of crossing, bends, and path length. An MMI splitter/combiner has 3.5 dB loss where 3 dB is due to 3 dB power splitting, and 0.5 dB includes component reflections [15]. Each path has 6 MMI splitters/combiners, and hence 21 dB signal loss is considered for each path. The path-dependent component loss contributions are approximated as 0.25 dB per wave-guide crossing [14], 0.2 dB per wave-guide bend [16], and 3 dB/cm of waveguide [14]. Coupling losses are determined experimentally by using in-/output SOAs as a photodetector and measuring photocurrents.

Figure 2(a) plots the number of components versus the path length. As the path length increase, the chance that the waveguide crosses other waveguides also increase. However, the longest paths are routed on the freer part of the chip, and the number of crossing is slightly low again. The loss contribution of each component for the paths arranged in ascending order of path length is shown in Fig. 2(b). As it stands out from the curve, the loss pattern follows that of the waveguide crossing, which indicates the number of crossings profoundly influences the path-dependent loss. Crossing contributes up to 24.5 dB loss on the worst path and 14 dB loss on average, contributing about 73 % of the path-dependent losses on average. The gain provided by three SOAs in a path has managed to compensate losses contributed by the MMI, waveguide bends fully, and waveguide length and some of the loss added by the waveguide crossing: 3 paths, in fact, show net on-chip gain.

Finally, the ER and OSNR of the optical switch are measured on the OSA when the SOAs are set to 70 mA and switching on/off the middle SOA. An example is shown in Fig. 2(d) for a representative path (6to3), with the blue line showing the output spectrum when the middle SOA is on and the red line presenting the output when it is off. It has demonstrated an OSNR and ER as high as 42.4 dB and 37.6 dB, respectively.

4. CONCLUSIONS

In this paper, we demonstrate an ultra-compact 8×8 InP photonic integrated switch fabricated with generic technology. The gain provided by three SOAs in each path has managed to compensate for the inevitable inherent loss due to the 3 dB MMI splitter/combiner used for the broadcast showing net on-chip gain for some of the paths. For the investigated chip, the number of crossing per path is moderate, leading to the high percentage contribution of path-dependent loss. Significant loss minimization is possible by optimizing the routing of paths and waveguide crossing component design.

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