The path to 1Tb/s and beyond datacenter interconnect networks: technologies, components and subsystems

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ABSTRACT

Modern IoT and 5G applications are driving the growth of Internet traffic and impose stringent requirements to datacenter operators for keeping pace with the increasing bandwidth and low-latency demands. At the same time, datacenters suffer from increasing number of interconnections dictating the deployment of novel architectures and high-radix switches. The ratification of 400 GbE standard is driving the market of optical transceivers nevertheless, a technology upgrade will be soon necessary to meet the tremendous traffic growth. In this paper, we present the development of 800 Gb/s and 1Tb/s optical transceivers migrating to 100 Gbaud per lane and employing wafer-scale bonding of InP membranes and InP-DHBT electronics as well as advanced co-packaging schemes. The InP membrane platform is also exploited for the development of novel ultra-fast optical space switches based on a modular architecture design for scaling to large number of I/O ports.

Keywords: datacenter interconnects, photonic integration, co-packaged optics, wafer-bonding, InP membranes, InP-DHBT electronics, 1Tb/s transceivers, optical space switches.

1. INTRODUCTION

Datacenter network traffic is experiencing steep growth reaching 25% every year, with the majority of this traffic concerning intra-datacenter, east-west communication[1]. To keep pace with traffic evolution, datacenter equipment providers are set on a two-year upgrade cycle, doubling the throughput of their network switches in every iteration. As current technologies are reaching their limits and in view of scaling to 51.2 Tb/s and beyond, there is growing consensus that new integration concepts are needed to sustain bandwidth growth, demarcating the end of pluggable modules and the beginning of the new era of co-packaged optics. In this new paradigm shift, electro-optic transceivers are co-packaged with the switch ASIC and essentially merge into a single product in the form of a co-packaged switch. Several demonstrations of co-packaged optics are reported, underpinning the strong commercial interest but also highlighting the outstanding technological challenges for moving to co-packaged switches[2]-[4]. At this stage there is no globally followed standard covering co-packaged optics, however the recently formed standardization groups aim to fill this void such as the Co-Packaged Optics Collaboration (CPO)[5] championed by Facebook and Microsoft, OIF Co-packaging Framework IA Project[6] and COBO co-packaged optics working group[7].

The growth of Internet traffic and the advent of modern time-sensitive applications also impose critical challenges to the interconnection of the datacenter resources which is more pronounced within the datacenter boundaries. As the datacenters grow in size the number of end-point connections grow as well dictating the use of high radix and low latency switches. Optical switches can overcome the bandwidth bottleneck and offer a transparent and power-efficient solution compared to their electronic counterparts. Optical architectures based on micro-electro-mechanical switches

(MEMS) and wavelength selective switches (WSS) have been proposed even with large number of input/output (I/O) ports, however, exhibiting tens of microseconds of switching speeds[8]-[12]. Faster optical switch architectures employ integrated technologies based on arrayed waveguide grating routers (AWGR) and semiconductor optical amplifiers (SOAs) providing nanosecond-scale switching[13]-[16].

In this communication, we report on novel reference architectures and components for the realization of 800 Gb/s and 1.6 Tb/s co-packaged optical transceivers for datacenter interconnects targeting 2, 10 and up to 40 km distances and ultra-fast optical space switches for intra-datacenter connectivity.

2. SCALING TRANSCEIVER CAPACITY TO 1.6T

The typical architecture of a co-packaged optics switch is shown in Figure 1(a). The switch ASIC is split into a core digital chip surrounded by satellite analogue/optical tiles that interface with the switch ports and thus with the outside world. In this concept the switch digital core and the optical tiles are assembled on the same substrate, thus forming a multi-chip module (MCM).

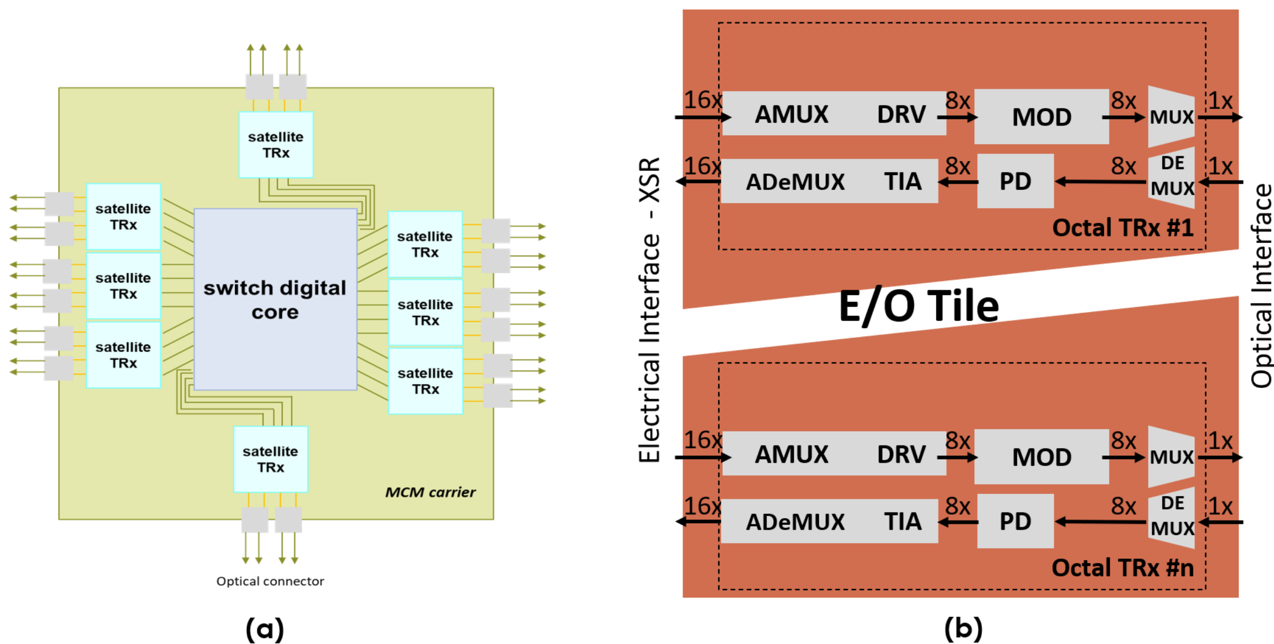

Figure 1. (a) Typical architecture of switch Multi-Chip-Module (MCM) with co-packaged optics, (b) conceptual block diagram of satellite transceiver (TRx) enabled by octal 1.6 Tb/s transceiver chips.

A single digital ASIC is surrounded by eight satellite transceivers to escape the entire bandwidth of the ASIC. The ASIC operates at 100 Gb/s per lane, therefore each electrical lane between the switch ASIC and the satellite transceivers is a 100 Gb/s PAM4 connection. A 25.6 Tb/s switch would provide 256 electrical lanes distributed to the 8 satellite transceivers, with each transceiver hosting 32 lanes (3.2 Tb/s bidirectional traffic). Upgrade to a 51.2 Tb/s switch would double the number of electrical lanes assuming 100G SERDES is still used, hence requiring optical satellites hosting 64 lanes (6.4 Tb/s bidirectional). Using current state-of-the-art 100 Gb/s technology this would require 64 individual transceivers, resulting in 128 fibers for 400GBASE-DR4 parallel single mode optics or 32 fibers for 400GBASE-FR4 CWDM optics. What is more, if external CW lasers are used, as in the case of silicon photonics solutions, additional fibers would be needed for delivering the CW light to the transceivers (a reasonable assumption would be 1 fiber for 4

lanes, adding 16 more fibers). The massive amount of fiber I/Os is a packaging hurdle combining optical and mechanical challenges compromising yield and loss uniformity.

In TWILIGHT project, advanced electrical and optical multiplexing are proposed to combat this issue. Figure 1(b) illustrates the conceptual block diagram of a satellite transceiver comprising of multiple electro-optic transceiver chips (E/O tiles). At the transmitter side, analog multiplexing (AMUX) is used for interleaving two 100 Gb/s electrical lanes into a single 200 Gb/s lane which then drives the optical modulator. At the receiver side, analog demultiplexing (ADeMUX) is employed for de-interleaving the 200 Gb/s electrical signal to two 100 Gb/s streams, respectively. Before the modulated optical signal is transmitted/received to/from the fiber, optical multiplexing/demultiplexing is performed on the photonic chip, resulting in 2 fibers per transceiver chip. Furthermore, the TWILIGHT photonic chip platform also hosts the lasers saving I/Os for light delivery. Optical multiplexing of 8 wavelengths yields 1.6 Tb/s transceiver chips and in total 8 fiber I/Os for a 6.4 Tb/s satellite transceiver which is within the current manufacturing capabilities. In the next subsections, the enabling photonics and electronics technologies that allow scaling to larger switch capacities are described.

2.1 InP membrane photonic integration platform

Indium Phosphide (InP) membrane photonic integration circuit (PIC) technology platform is known for its high index contrast and strong optical confinement which is achieved by removing the InP substrate yielding significant speed performance benefits. Selective area growth (SAG) in combination with butt-joint process allows to obtain a wide range of optical emission wavelengths in a single chip and at the same time a low-loss and low-reflection active-passive interface[17]. Moreover, tight optical S-bends can be realized enabled by optical quality vertical etching in InP membrane platform with much reduced bending radii as compared to substrate InP platform. The high numerical aperture of the membrane waveguides offers the possibility of using corner mirrors to achieve extremely small footprints for this function, allowing very dense photonic circuits. In generic InP PICs this idea is not so effective, because the losses are highly sensitive to a vertical tilt of the mirror, but in membranes this sensitivity is much reduced due to the high numerical aperture. Ultra-low loss (0.13dB/90 degrees) for miniaturized bends (effective radius 0.96μm) has been demonstrated on the InP membrane platform based on a cavity designed around the mirror[18]. Besides the apparent benefits in footprint and PIC miniaturization, scalability to larger transceiver array is inherently feasible in PIC platforms relaxing the need for continuously increasing the lane rate to achieve larger transceiver capacities.

The envisioned 1.6 Tb/s transceivers employ the InP membrane platform for the development of the optical components used for signal generation, detection, amplification and optical multiplexing of the parallel optical lanes, thus forming a compact system-on-chip photonic circuit integrating multiple signal processing functionalities. The first transmitter and receiver modules will rely on quad arrays of photonic components and electronic ICs yielding a total output of 800 Gb/s targeting the next 800 GbE standard which is anticipated before the ratification of 1.6 TbE. Migration from 800 Gb/s to 1.6 Tb/s transceivers will rely on the same generation of photonics and electronics components and it will be achieved by doubling the array size and developing octo-chips (Figure 1(b)).

The mainstream photonics technology for the datacenter interconnect market is the use of Directly Modulated Lasers (DMLs) and Electro-Absorption Modulated lasers (EMLs) with the former to be better suited for shorter distances (i.e. 100m-500m) due to their inherent limitations stemming from direct modulation and the latter to comprise a robust solution for 2 km, 10 km and up to 40 km with enhanced digital signal processing (DSP) chipsets. Currently, 56G EML technology is employed in the second generation of 400 GbE pluggable modules exploiting 4 optical lanes. Scaling to 800 Gb/s is possible using 8 optical lanes but to scale to 1.6 Tb/s migration to 100G EML technology is necessary (i.e. 100 Gbaud per lane), considering the scalability constraints discussed in the beginning of section 2. The novel transceivers will comprise distributed-feedback traveling wave electrode electro-absorption modulated lasers (DFB-TWEAMs) with segmented electrode sections for achieving 100 GHz bandwidth and high-speed operation. Such a design has demonstrated record performances as stand-alone devices reaching up to 200 Gb/s based on on-off-keying (OOK), 4-level pulse amplitude modulation (PAM4) and discrete multitone (DMT)[19]-[22] and will be transferred to InP membrane platform. Figure 2 depicts the segmented electrode EML design and the attained 3-dB bandwidth achieved as a standalone device from previous developments. SAG and butt-joint process will be used to independently engineer the bandgap of every single EML transmitter to match to the specific wavelength grid of the overall array (quad- and octo-array). The transceivers will address both intra- and inter-datacenter connectivity and for this reason both O-band and C-band EML arrays will be developed. SAG will be exploited to develop the active laser layer and the modulator layer in a

single process growth step. The use of an integrated semiconductor optical amplifier (SOA) will be investigated for achieving the necessary output power for the respective target datacenter use case.

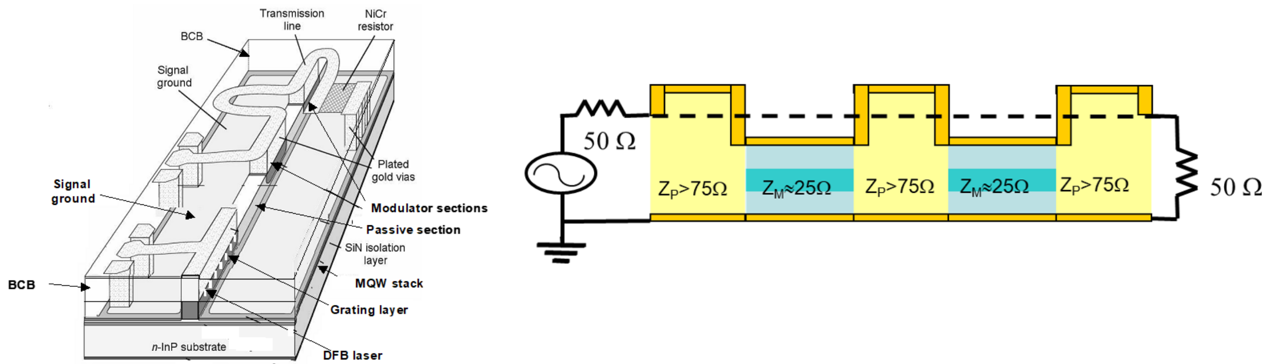

Figure 2. DFB-TWEAM design with segmented electrode sections[24] to be transferred to InP membrane PIC platform.

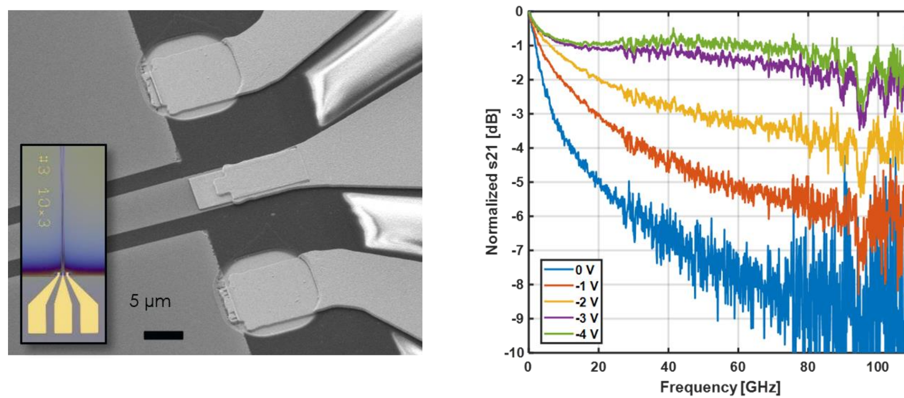

Figure 3. (left) SEM image of the UTC photodiode on InP membrane platform. (right) S21 measurements of the device.

At the receiver, high speed uni-travelling carrier (UTC) photodiodes (PDs) will be developed intrinsically operating at the C-band and at the O-band. Recent measurements on membrane UTC-PDs reveal 3-dB bandwidth beyond 110 GHz at a bias voltage in the range of -3 to -4 V bias, as shown in Figure 3. The responsivity of the device is 0.25 A/W, due to the ultrasmall footprint of 3x2 μm^2 and it can be increased by reducing the loss induced by metal contacts. Improvement of the bias voltage at the level of -1V will be pursued via optimization of the layerstack. Polarization insensitive semiconductor optical amplifiers (PI-SOAs) will be considered at the receiver front-end in order to amplify the received signal especially for the transceivers targeting 10 km and beyond transmission distances. Polarization insensitivity is naturally obtained for SOAs using the bulk InGaAsP gain medium eliminating the need for polarization handling elements that will increase the circuit complexity of the photonic chip. The PI-SOAs will be used for the development of the optical space switches discussed in section 3. Optical multiplexing and demultiplexing at the transmitter and the receiver side will be accomplished by means of arrayed waveguide gratings (AWG) appropriately designed to ensure low loss and minimum channel crosstalk.

2.2 InP-DHBT electronics

Analog time-domain electrical multiplexing and demultiplexing is becoming of crucial importance for further increasing the symbol rate of datacenter and optical metro transmission systems (provided that the photonics components can also

support it). The proposed 1.6 Tb/s transceivers exploit 0.5-µm InP-DHBT technology for developing high speed and compact electronic integrated circuits (ICs) which will interface with latest 112 Gb/s SERDES and will enable 100 Gbaud per lane.

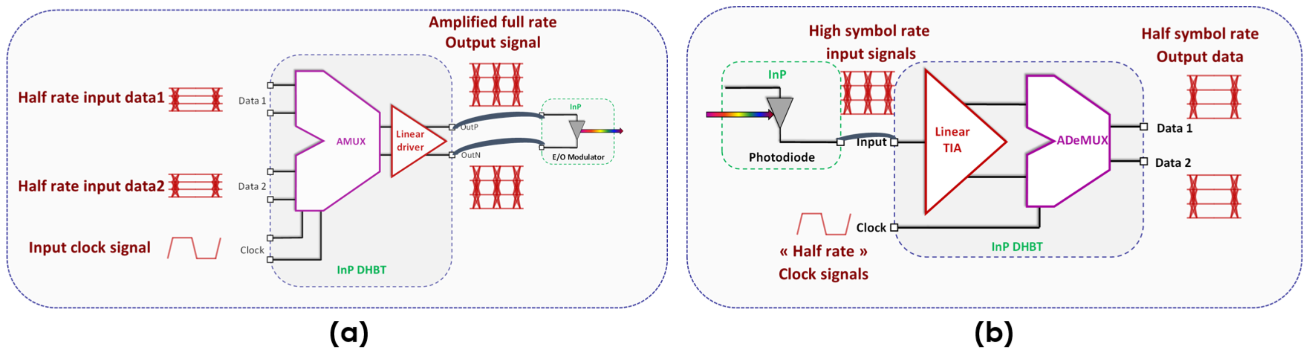

Figure 4. (a) Operation principle of transmitter InP-DHBT electronics ICs, (b) Operation principle of receiver InP-DHBT electronics ICs.

As depicted in Figure 4(a), the analog multiplexer (AMUX) receives the two 100 Gb/s input data streams (50 Gbaud PAM4) together with a 50 GHz clock signal and multiplexes the two 100 Gb/s tributaries to a 200 Gb/s electrical data stream. A linear driver is then used in order to amplify the 200 Gb/s signal and to provide sufficient drive voltage to the EAM to maximize the optical extinction ratio. Recent work has demonstrated good performances for the AMUX at 70 Gbaud and 100 Gbaud for PAM4 signals showing $1V_{pp}$ and $0.9V_{pp}$ differential output voltage, respectively[25]. A linear InP-DHBT driver with $3V_{pp}$ differential output swing at 80 Gbaud using PAM4 modulation was also demonstrated[26]. The driver chip exhibits 106 GHz bandwidth and peaking gain of 5.7 dB at the high frequency range allowing to compensate for potential bandwidth limitations of the optical modulator, hence extending the overall transmitter bandwidth. In the novel 800Gb/s and 1.6 Tb/s optical transceivers the analog multiplexing and amplification functionalities will monolithically be integrated into a single AMUX-linear driver chip targeting an over 100 GHz 3-dB bandwidth and a 1.5 V_{pp} linear output swing.

The transmitted 200 Gb/s optical signal is detected at the optical front-end of the receiver and it is converted to electrical after the high speed photodiode, as illustrated in Figure 4(b). It is then amplified by the high speed transimpedance amplifiers (TIAs) and it is fed to the analog demultiplexer (ADeMUX) circuit. The ADeMUX will receive the two outputs of the TIA as well as a 50 GHz clock signal and will output the two tributaries each at 100 Gb/s. Likewise at the transmitter, also at the receiver, the analog multiplexing and TIA functionalities will be monolithically integrated into a single ADeMUX-TIA chip. The TIAs will exhibit more than 100 GHz 3-dB bandwidth and very high linearity (total harmonic distortion (THD) <5%) for distortion-free detection of high speed PAM4 signals. Preliminary measurements of test TIA chips at 50 Gbaud using PAM4 modulation show good performances and 360mVpp linear output voltage swing. The 800Gb/s and the 1.6 Tb/s optical transceivers will rely on quad- and octo- two-dimensional arrays of the electronics transmitter and receiver circuits, respectively.

2.3 Co-integration of photonics and electronics and development of system-in-package (SiP) transceivers

Figure 5 illustrates the assembly concept of the proposed transceivers. Co-integration of InP membrane photonics and InP-DHBT electronics layers is performed at wafer-level via a polymer multilayer (Benzocyclobutene, BCB). Polymer-based bonding technology ensures high tolerance to complex topologies in processed photonics and electronics wafers and it is flexible to a wide range of chip and wafer sizes. The thickness of the polymer bond layer between the photonics and electronics layers will be 10-20 µm and their interconnection will rely on high speed and high-density through-polymer vias. Sloped via interconnections have been previously developed[27], showing no signal decay at high speed up to 67 GHz and further simulation work ensures 100 GHz speed. In this new effort, vertical vias will be exploited with metallic atomic layer deposition (ALD) technology aiming for a factor of 10 reduction in via footprint (from hundreds of µm to tenths of µm). With the photonics and electronics co-integrated into one wafer, and interconnected through ultra-

short vias, the parasitics commonly seen in traditional hybrid assembly techniques are significantly reduced. This enables high speed and low energy operation of the co-integrated devices, since the signal attenuation during transportation is much less pronounced in short interconnection distances (tens of µm based on wafer-scale co-integration concept instead of tens of mm in traditional wire bonding assembly).

Besides the speed and efficiency advantages, the material and process compatibility play a crucial role. The InP photonic membrane and the InP-DHBT electronics share the same material system and thus, the two functional layers experience zero expansion mismatch at the wide process temperature range (e.g., from room temperature to 300 °C in plasma processes). With zero mismatch, the alignment accuracy between photonic and electronic layers can be pushed down to the tool limitation (1 µm). On the contrary, integrating InP chips or membranes on SiGe CMOS is confronted with significant thermal expansion mismatch (InP: 4.6×10^{-6} °C^{-1}; Si: 2.6×10^{-6} °C^{-1}), which as a result limits the alignment accuracy between the two layers to the order of 10-20 µm over the wafer scale. Such material compatibility is also beneficial to field applications. It is noteworthy that in datacenters the temperatures can reach 80 °C which may cause the co-integrated system to experience stress due to thermal mismatch; yet, the InP membrane – InP-DHBT co-integrated system will experience minimum thermal stress exhibiting longer lifetime and higher reliability in harsh operating environments.

The high-density vertical vias will be also exploited for thermal management at wafer-scale. Co-design of the photonics and the electronics layers must be carefully considered in order to ensure optimum performances. Thermal studies will be carried out to produce heat maps of the whole photonics/electronics cross section. Thermal vias will conduct heat from the photonics membrane to the electronics wafer which will be cooled with a heat sink. Additional thermal management will be considered at the module level i.e. active cooling by means of a thermo-electric controller (TEC). The optoelectronic chip is interconnected to the switch ASIC by means of high-speed RF lines on a common substrate (high speed multi-layer PCB). Programmable current/voltage sources for driving the various photonics and electronics components of the transceivers are placed on the host PCB as well. Detailed thermal studies will be carried out for the overall transceiver assembly concept in order to define the appropriate interposer and high-speed PCB materials and the bonding process parameters.

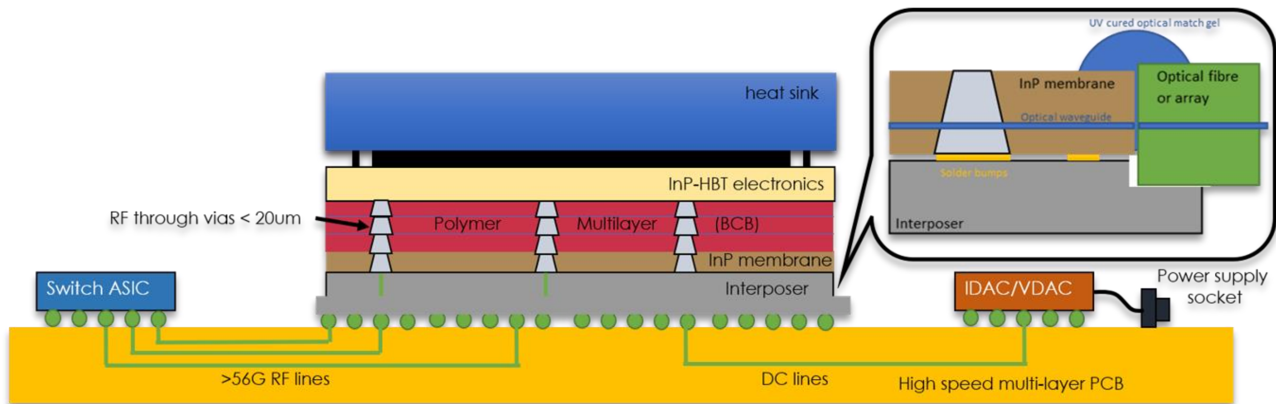

Figure 5. Concept of system-in-package (SiP) transceivers and co-packaging with ASIC chip. Programmable current/voltage sources (IDAC/VDAC) are placed on host PCB for driving the various photonics and electronics components.

Figure 6 shows a schematic illustration of the co-integrated layerstack of the InP membrane photonics and InP-DBHT electronics layers with the BCB bonding layer in between. Critical parameters for the co-integration are surface topology, maximum temperatures tolerated, the thickness of the substrate and the sample size. Currently, thermal bonding tests are being carried out for defining the optimum bonding parameters. The 800 Gb/s transmitter and receiver modules will rely on the co-integration of reticles and the 1.6 Gb/s transceivers will rely on the co-integration of full 3-inch wafers.

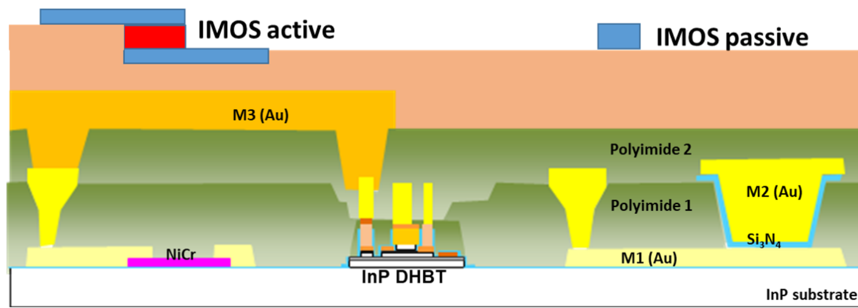

Figure 6. Schematic illustration of the co-integrated InP membrane photonics and InP-DHBT electronics layerstack.

3. ULTRA-FAST HIGH RADIX OPTICAL SWITCHES

SOA-based architectures employ SOAs as the basic switching element that defines the most critical properties such as switching speed, insertion loss, power consumption, polarization dependent loss and on/off ratio which are influenced by the SOA design. Nevertheless, the way that the basic switching elements are connected together play a crucial role in the overall switch architecture performance. Modular architectures differ in parameters such as the number of switching elements, the total number of SOAs, number of SOAs in a path, number of switching stages, number of crossovers resulting in different path loss, blocking or non-blocking property, footprint and overall power consumption. Two reference architectures will be considered for the development of the optical space switches demonstrating the capability to implement different modular designs on the same photonic platform simply by re-arranging the topology of the basic switching blocks. The first reference switch architecture is inspired by OPERA datacenter architecture[28]. OPERA requires a single layer of optical switches with multiple I/O ports for implementing a predetermined set of matchings (shift permutations) and interconnecting the top-of-rack (TOR) switches. Moreover, the routing rules are implemented on the TOR switches shaping the traffic at the network state i.e. it relies on decentralized control implying that a centralized controller in not required. The second reference datacenter architecture is based on OPSquare[29] which relies on centralized control and two levels of optical switches. An intra-cluster optical switch network which interconnects a limited number of TOR switches that exist in the same cluster (1 hop) and an inter-cluster optical switch network that interconnects a TOR switch from one cluster to a TOR switch of another cluster (maximum 2 hops). OPSquare would thus require optical switches with a small to medium number of ports but ultra-fast switching times.

The PI-SOAs that will be developed on the InP membrane platform will also be exploited for the development of 4x4 and 16x16 optical space switches providing nanosecond switching times stemming from the ultra-fast gain recovery for the SOAs. Various topologies will be investigated considering the critical parameters described above and a modular design in combination with the physical performance of the basic switch element. The assembly approach for the optical space switch is similar to the optical transceivers described in Figure 5 with the difference that there is no InP-DHBT electronics layer present (neither the multilayer bonding layer). An interposer will also be used here as well for mechanical stability. Programmable current/voltage sources are placed peripheral to the optical switch chip on the host PCB for driving the PI-SOAs. The interconnection of the interposer on the host PCB will be based either on RF lines or wirebonds considering a number of parameters including the total number of SOA connections, the pad layout and overall thermal performance as well as the latency constraints for the reference architecture to be employed. The latter is mainly defined from the sum of the time the SOAs will switch from the “on” state to the “off” state and vice versa and the time for reconfiguring their state by means of the control electronics circuit. All the above key parameters will be taken into account for the design of the novel all-optical space switches.

4. CONCLUSIONS

In this paper, we propose a novel reference optical transceiver architecture enabling the migration to 800 GbE and 1T based on a single technology upgrade step and novel co-integration and assembly methodologies. For this new type of

co-packaged switches, InP membrane photonics and InP-DHBT electronics technologies are employed and are brought together via wafer-scale bonding at unprecedently close distances ensuring signal integrity and high-speed operation. Arrays of the high-speed segmented DFB-TWEAMs and UTC photodiodes with 100GHz 3-dB bandwidth comprise the core of the optical engine. On-chip optical (de)multiplexing reduces the number of I/O fibers and relaxes the packaging complexity allowing the realization of scalable high capacity switches. On the electronics side, analog (de)multiplexing is used to interface with current 100G electrical interfaces migrating to 100 Gbaud per lane. Linear amplification will be monolithically integrated on the InP-DHBT transmitter and receiver ICs (linear drivers and TIAs). Furthermore, novel ultra-fast optical space switches on the membrane platform are proposed based on polarization insensitive SOAs as the basic building block. Reference switch architectures will be implemented exploiting a modular approach relying on the OPERA and OPSquare datacenter architectures.

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