Towards wafer-scale integration of InP membranes on 3" InP substrates for next-generation 1.6Tb/s optical transceivers

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Herein we present a general outlook on the challenges faced towards wafer-scale co-integration of InP electronics and InP membrane-based photonics. We then investigate the thermal budget limitation on the InP ICs that is imposed by the wafer bonding process. We also discuss preliminary investigations of post-bonding alignment accuracy and its implications on pre-bonding processes and co-design of the mask layout.

Introduction

Responding to the rapid growth of demand on datacenter traffic, the TWILIGHT project aims to demonstrate next-generation transceivers for ultra-high speeds and lower power consumption [1]. It is proposed to realize wafer-scale co-integration of InP membrane-based photonics [2] and InP high-speed double heterojunction bipolar transistor (DHBT) electronics to drive them [3]. Here, co-integration via adhesive bonding allows for combining the high-speed devices from both worlds with high tolerance over the surface topographies, and creating short through-polymer-via interconnects (vias) to intimately connect them at distances below 20 μm. The aim is to reduce parasitic effects and integrate a higher density of devices and interconnects on-chip. This concept has been pioneered on BiCMOS wafers [4]. We discuss in this paper the challenges that arise from co-integration with InP electronics and the ongoing work to tackle them. We first assess the thermal budget limitation of InP HBTs and its implication on the bonding and post-bonding processes. We also discuss issues related to post-bonding alignment accuracy and the relevant methods to improve it. Finally, we investigate polymer resists for selective wafer etch-back for membrane processing.

Co-integration technology

TWILIGHT aims to co-integrate fully processed electronics with semi-processed photonics via adhesive wafer bonding using BCB polymers [5]. The stack is then post-processed after bonding to complete the functional photonic devices and create interconnections between photonics and electronics layers. Bonding of high topography wafers has been previously investigated and demonstrated on BiCMOS wafers [6]. It was determined that a thickness of BCB equivalent to double the topography is necessary for planarization and void-free bonding, which translates to a high thickness above 12 μm in our case, the latter being dominated by the high topography of InP DHBT wafers (about 6 μm).

Moreover, full cross-linking of BCB is required for mechanical and chemical stability, whereby the stack is cured for multiple hours depending on the curing temperature [7]. The required thermal treatment for this can deteriorate the transistors' performance during bonding. Therefore, the next section is dedicated to finding out the thermal budget

limitations imposed by the InP DHBTs to avoid applying high temperature and/or for extended times during the bonding (and post-bonding processes).

Thermal budget assessments of InP electronics

Here, we systematically study the effects of thermal treatment on InP electronics. For this purpose, high-speed (> 350-GHz f_T) DHBTs with 0.7×5µm² and 0.7×10µm² emitter sizes were fabricated by III-V Lab [3]. Each chip contained a total of 24 InP DHBTs that were measured before and after treatment for comparison.

The treatment process was carried out in the chamber of the EVG wafer bonder at a high vacuum ($<10^{-5}$ Torr) to simulate real bonding conditions. The BCB curing temperature, ramp rate, and curing time are varied to study the thermal budget. The treatment temperatures are 200, 240, 260, 280, and 300 °C. The full range of ramping rates and baking times were respectively chosen as 2, 5, and 10 °C/min (from room to target temperature), and 0.5, 1, 2, 5, 10, and 20 hours. To be precise, the exact ranges of these two last parameters were set considering the required thermal budget for full BCB crosslinking, and also based on the treatment temperature to stay within presumed safe conditions, given the possible rapid degradation of devices. Hence, higher ramping rates and baking times were investigated for low temperatures, and vice versa for higher temperatures. This comprehensive analysis yielded 24 process variations.

The DHBTs were measured at III-V Lab pre- and post-treatment. Their DC performance was assessed using $I_C(V_{CE})$ curves and Gummel plots at V_{BC} = 0 V, and their RF performance with S-parameter measurements up to 110 GHz. Subsequently, their post-processing functionality was determined based on the degree of degradation in series resistances (including the emitter resistance, R_E), as well the transition and maximum frequency oscillation (f_T and f_{MAX}) values.

All samples baked at 200 and 240 °C demonstrated satisfying DC characteristics. Regarding chips baked at 260 °C, most samples were still considered safe after thermal tests, whereas samples baked for 5 hours showed a slight degradation of their series resistances. For chips baked at 280 °C a slightly deteriorated performance was observed for baking times lower than 1 hour, whereas longer times led to strong degradations of series resistances as shown on Gummel plot at high V_{BE} values (> 0.85 V) and on I_C (V_{CE}) saturation slope (Fig. 1).

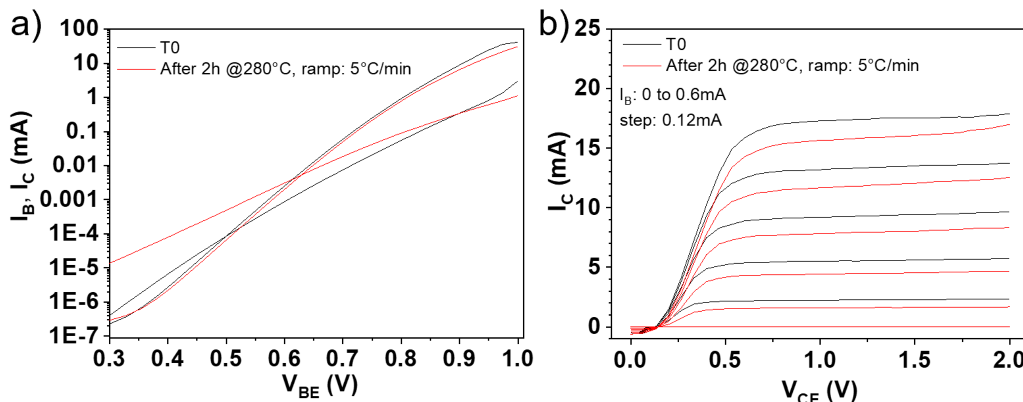

Figure 1: 0.7x5µm² InP DHBT DC characteristics before and after baking at 280°C during 2 h, ramp speed of 5°C/min

Finally, all devices baked at 300 °C were significantly degraded. Additionally, we observed no noticeable effect of the ramping rates in our experiments. Based on the

frequency performance and small-signal parameter analysis, we conclude that the performance degradation preliminary observed from DC measurements is essentially due to the emitter resistance degradation. R_E increases by more than 25% for samples baked at 260°C for 5 hours and 50% for those baked at 280 °C during more than 1 hour. Based on this, we capped the temperature of our bonding processes to 240 °C, whereas post-bonding processes can be limited up to 260 °C for less than 5 hours cumulatively if these are deemed necessary.

Post-bonding alignment accuracy

High post-bonding alignment accuracy is crucial for the fabrication of compact vias interconnections. In theory, a commercial wafer bond aligner can achieve an alignment accuracy of 1-2 µm [5]. However, several mechanisms affect the aligned wafer stack during the actual bonding process and lead to a deteriorated alignment. The eventual misalignment can exceed 100 µm, especially for very high thickness bonding layers [8], which is also the case of this work.

For BCB bonding of wafers with the same coefficient of thermal expansion and similar bow profiles, such as our case, misalignment errors result only from shifts (translations) in the (x,y) plane. The other distortions are not present. These are, rotations which are minimized in state-of-the-art tools, and expansion due to mismatch in the wafers' thermal expansion coefficients [5]. Shifts are often attributed to the presence of shear forces during the reflow state of BCB when the wafers are being bonded [8]. Consequently, a wafer-scale systematic shift is expected for similar bonding conditions depending on the value of shear forces and viscosity of BCB [8]. Hence, we carried out a systematic investigation of the misalignment mechanisms present in our bonding process. These will be discussed next along with the relevant potential solutions.

To simplify the bonding process, we start with 3" double-side polished fused silica transparent glass wafers. The bows of each wafer (< 20 µm) were measured beforehand and matched such that a convex post-bonding low bow profile is achieved with minimal distortions to the original bow shapes. The similarity in bow profiles also helps in reducing the thickness variations of the BCB layer, which are generally in the order of 10-20 %, thereby reducing the effect of this variation in our study. Next, 10/100 nm-thick Ti/Au alignment markers were fabricated, and a 40-nm SiO_2 layer was deposited as adhesion promotor for BCB. Subsequently, a standard BCB recipe (using Cyclotene 3022-57) was used to spin-coat a single 10-µm-thick layer [6]. A post-bonding thickness of about 9 µm was measured using a reference InP-on-Si sample after removal of the InP. The two wafers are then pre-aligned in EVG bond aligner and clamped into a cassette holder, then subsequently transported and bonded in the EVG bonder. The full experiment was repeated 3 times.

The wafer-scale average shifts we recorded for the three samples are (37, 2), (58, 12), and (13, 8) µm in (x,y) coordinates (Fig. 2.a). This indeed signifies a preferred directionality of the shifts resulting from shear forces, but it is also combined with a random shift effect responsible for the high scatter in values. The systematic shift may be attributed to an uneven clamping force of the cassette holder, since the clamping force was intentionally lowered to avoid cracking of the fragile InP wafers. It is worthwhile to note that these EVG bonder and bond aligner imperfections fall within its fabrication tolerances and cannot be improved. Therefore, we are currently investigating possible processing solutions to account for the consequent errors, which are briefly introduced here.

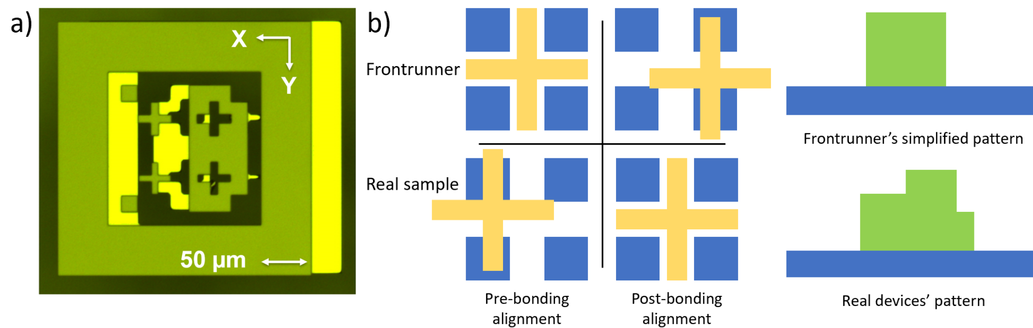

Figure 2 a) post-bonding misalignment from the first experiment. b) Illustration of the accurate pre-compensation process using a frontrunner

One way to overcome the systematic errors is to use frontrunner samples with the same bonding process and simplified patterns resembling the 3D shape of the actual device patterns and locations. The latter is done because the presence of patterns may restrict the reflow of BCB during bonding to a certain extent, which reduces the shift. Subsequently, an averaged shift of multiple frontrunners can then be used as a pre-compensation during the alignment of the real wafers (Fig. 2.b) [8].
However, this method does not influence the random shift, which is why the latter need to be taken into account in the co-design of the mask layout. This step comes into play when designing vias interconnections where precise openings are needed. Here, the size of the openings should take into account the value of this random shift.

Conclusions

The general requirements for wafer-scale co-integration of InP-electronics and InP-photonics have been discussed. Thermal budget assessment of the InP DHBTs' side was comprehensively studied. The bonding and post-bonding temperatures were capped to 240 and 260 °C for less than 5 hours to avoid accumulating thermal damage. We also discussed results on the alignment accuracy and possible methods to improve it.

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