



Photonic Integration on a Sub-micron InP Membrane

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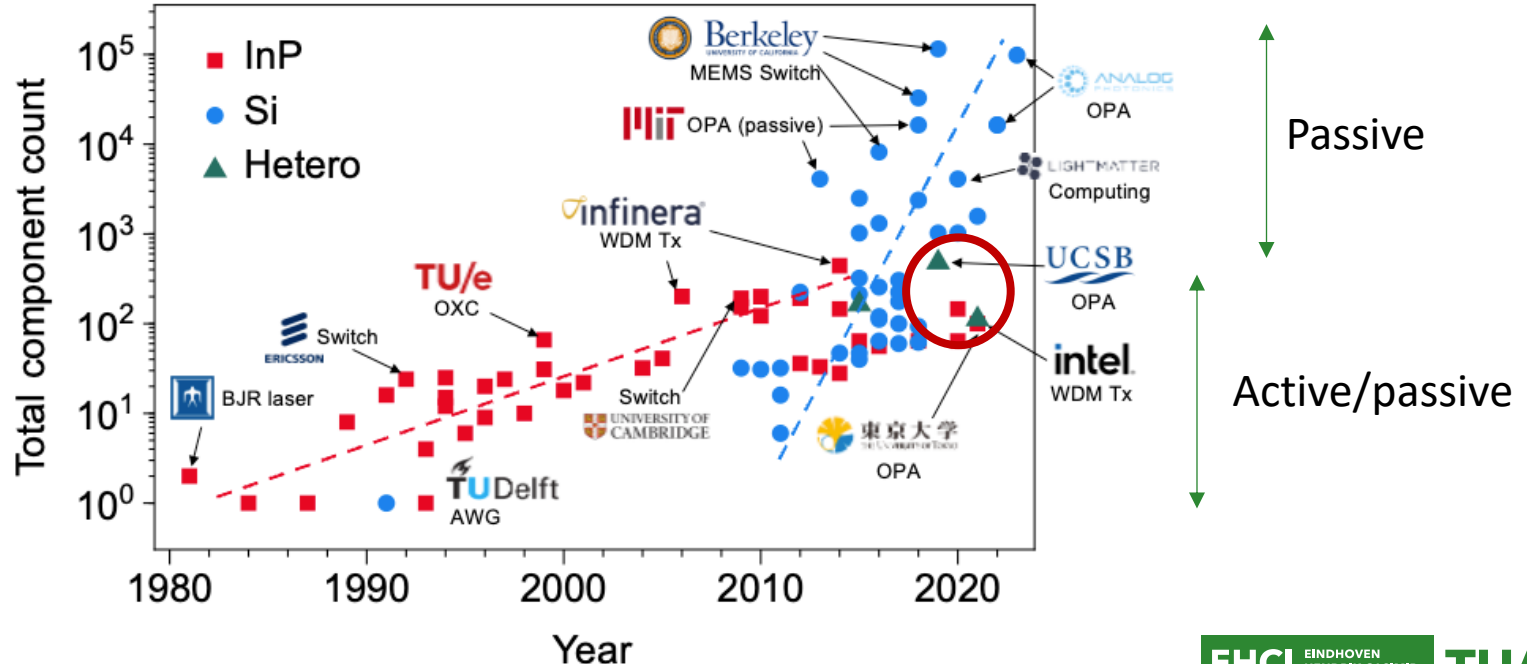
Electrical Engineering, Photonic Integration

Outline

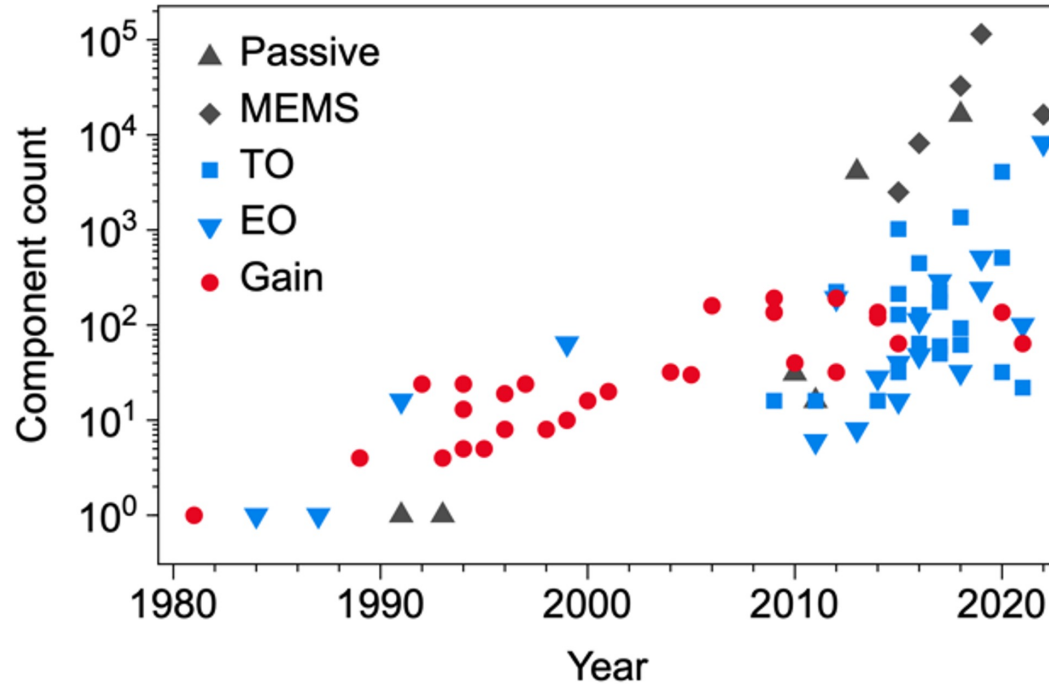
- Density bottleneck in photonic integrated circuits
- Our technology on an InP membrane
- Miniaturization and efficiency boost in active devices
- Summary

Photonic Integration

- Density bottleneck is not solved by introducing Si photonics alone
- Active components limit the density in heterogeneous circuits



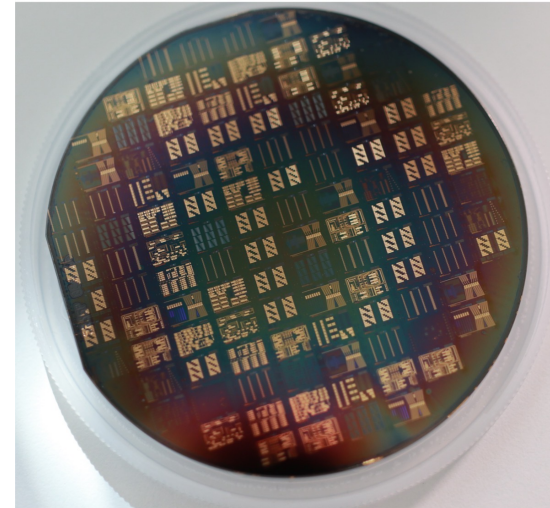
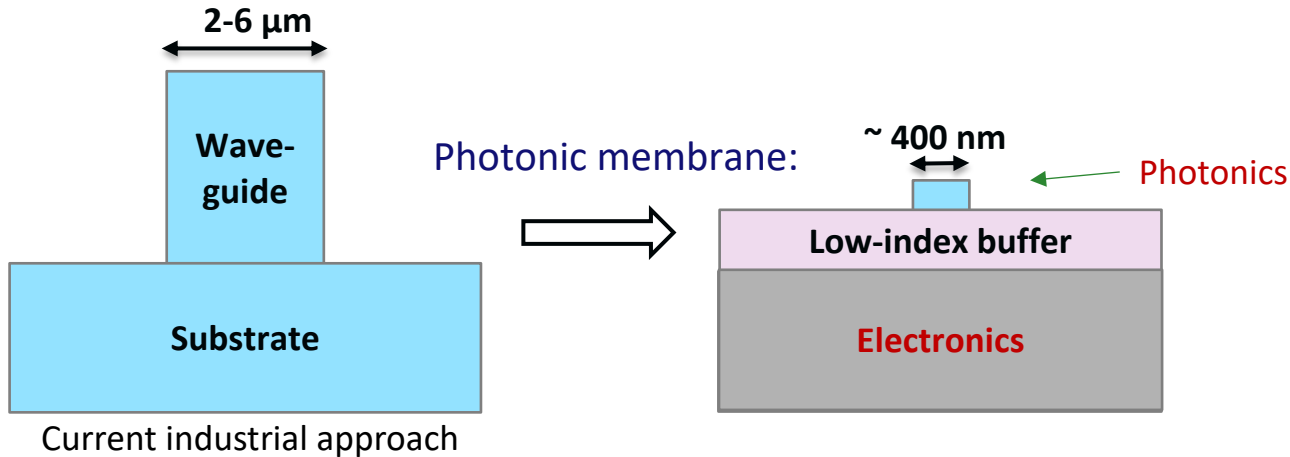
Photonic Integration



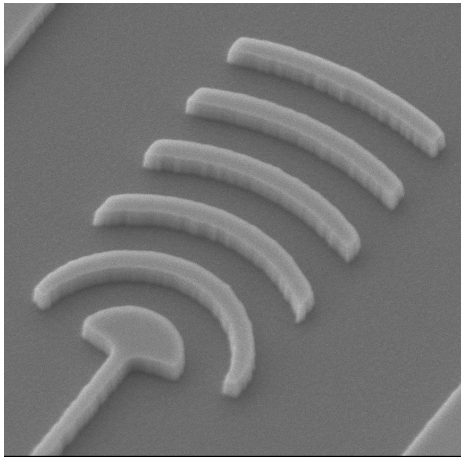
- Density boost driven by passives and MEMS optics
- Gain and EO elements remained relatively bulky

Photonic Integration in a membrane

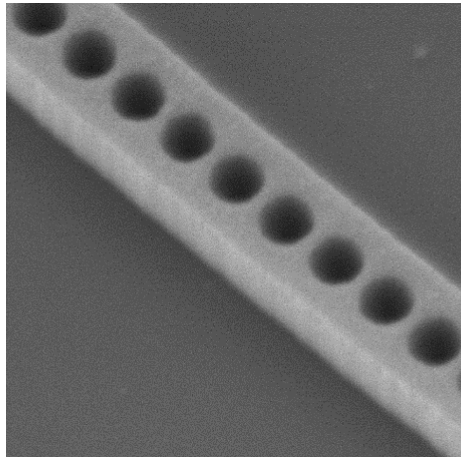
- InP membrane: InP amplifiers/lasers + SiPh-like nanowire waveguides
- Wafer-scale assembly with electronics



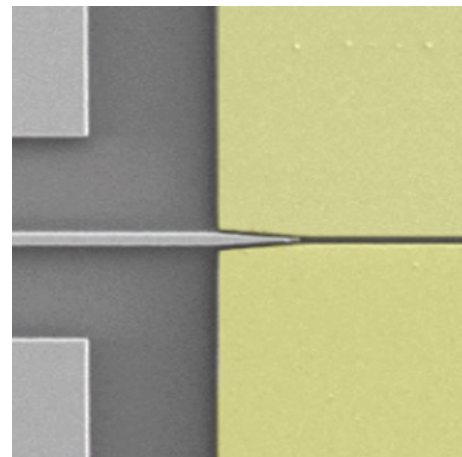
Nanophotonic passive library



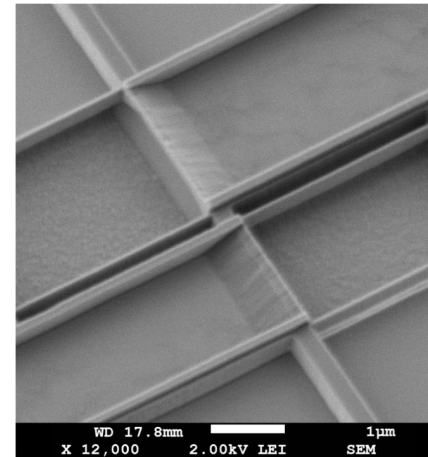
Grating antenna



Photonic crystal



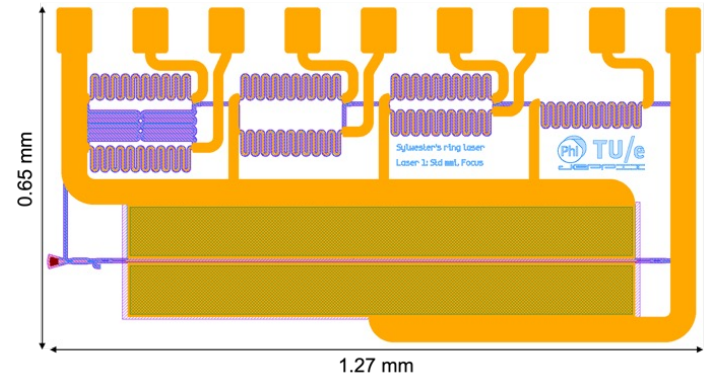
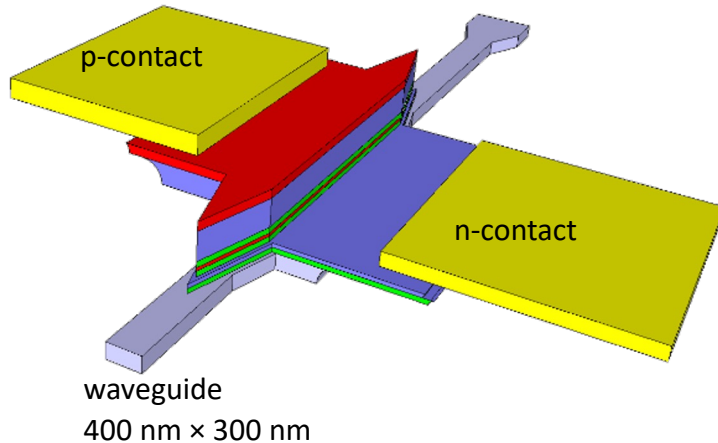
Plasmonics



Polarization rotator

Lasers on nanophotonic waveguides

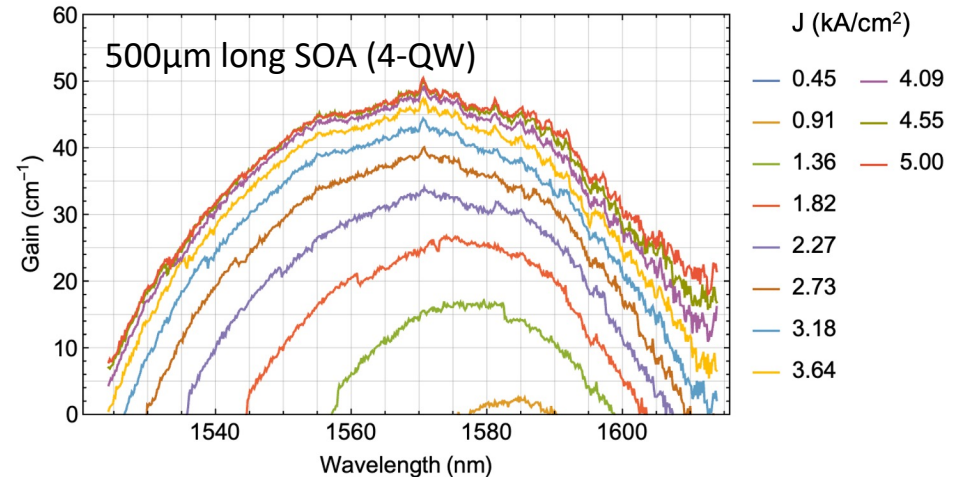
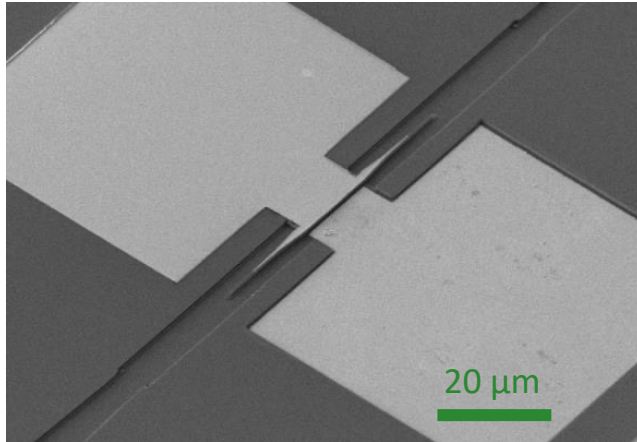
- S-shaped amplifier/laser for balanced confinement vs power handling
- Improve optical mode matching – very short tapers
- No critical alignment (lithography overlay accuracy)



Compact tunable laser on membrane
4x smaller than conventional designs in bulk InP

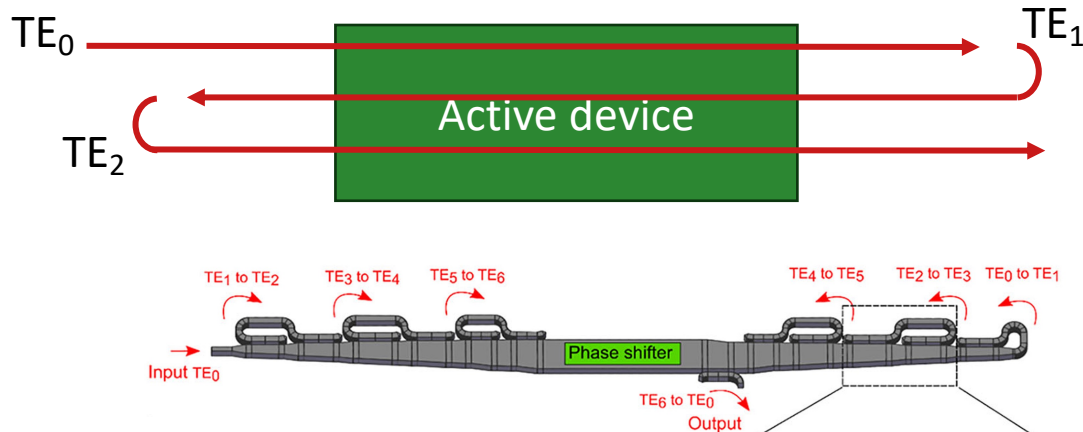
Amplifiers are intrinsically power hungry

- ~ 200 dB/cm net modal gain in 4-QW SOAs
- Wall-plug efficiency (WPE) typically $< 1\%$
- High electrical power supply to amplifier weak optical signals
- Improvements exist at device level: optimizing QW materials, electrical structure, etc



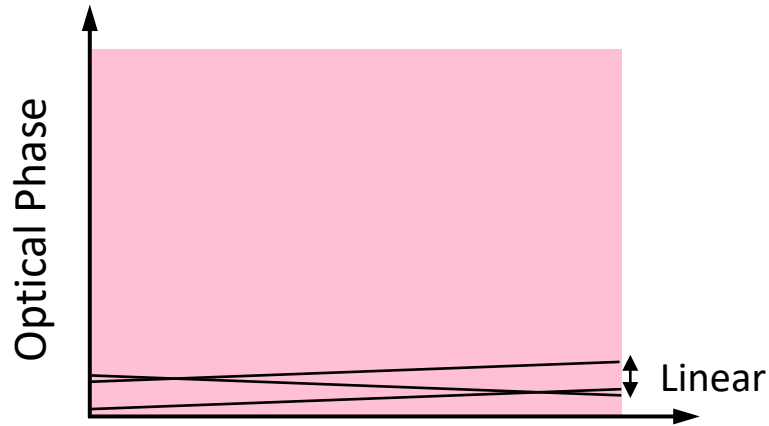
Circuit-level method: Folding the device by MDM

- Recirculation of the light multiple times
- Footprint benefit: a fraction of the length needed in single-pass design
- Efficiency benefit: a fraction of the energy consumption
- No resonance thanks to the use of orthogonal waveguide modes

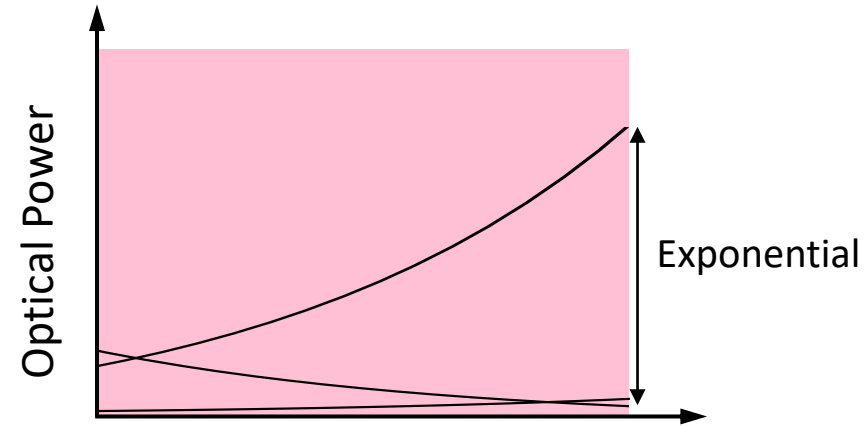


Recycling light in a phase shifter: Lipson, Optica 7, 3-6 (2020)

Multi-pass: linear vs nonlinear



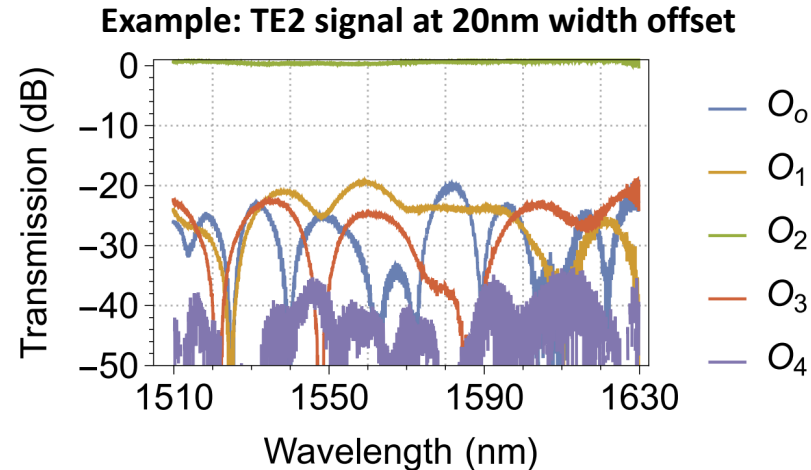
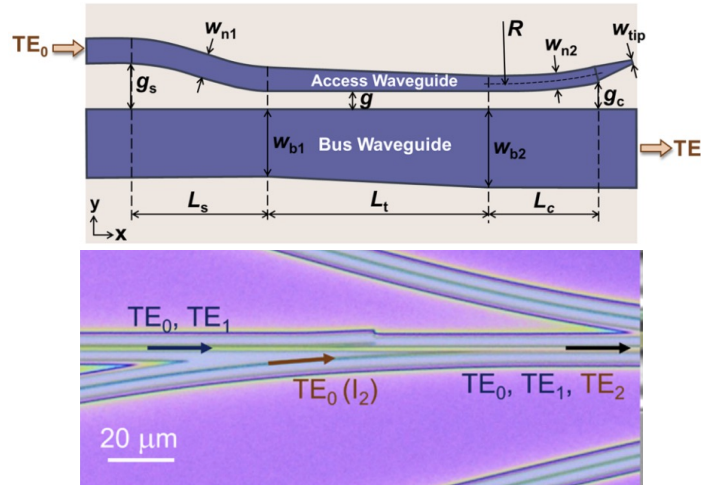
N-pass: N times enhancement



N-pass: \gg N times enhancement

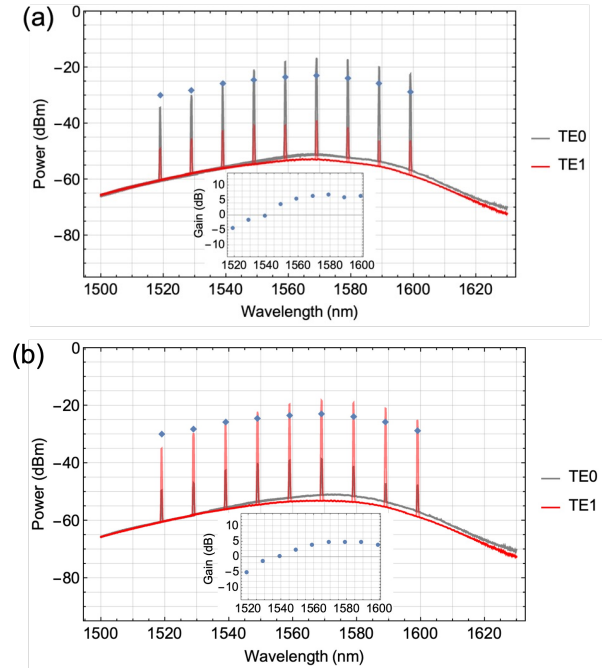
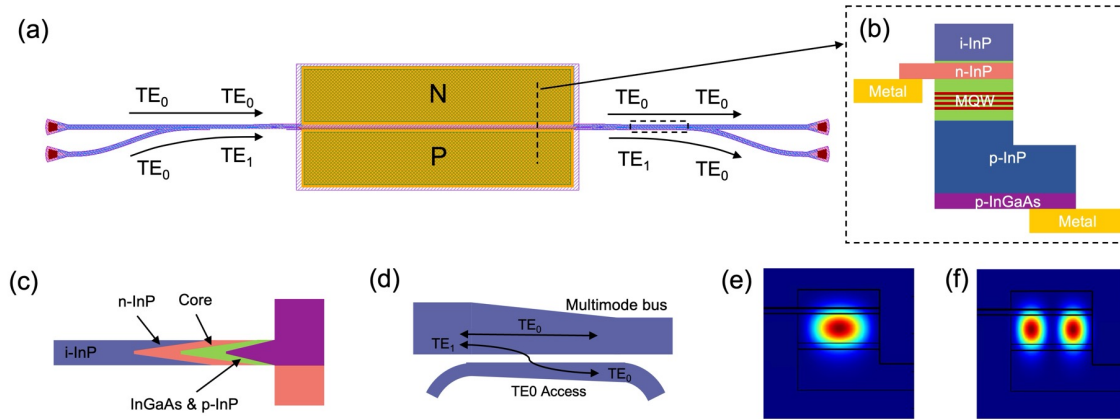
Fab tolerant mode (de)multiplexers in InP membrane

- First mode multiplexer (5 modes) on InP
- Broadband ($\sim 100\text{nm}$)
- $\text{EL} < 1\text{ dB}$, $\text{XT} < -14\text{ dB}$ with 50nm width variation
- InP offers high fab tolerance due to moderate index contrast



Mode multiplexing in membrane SOAs

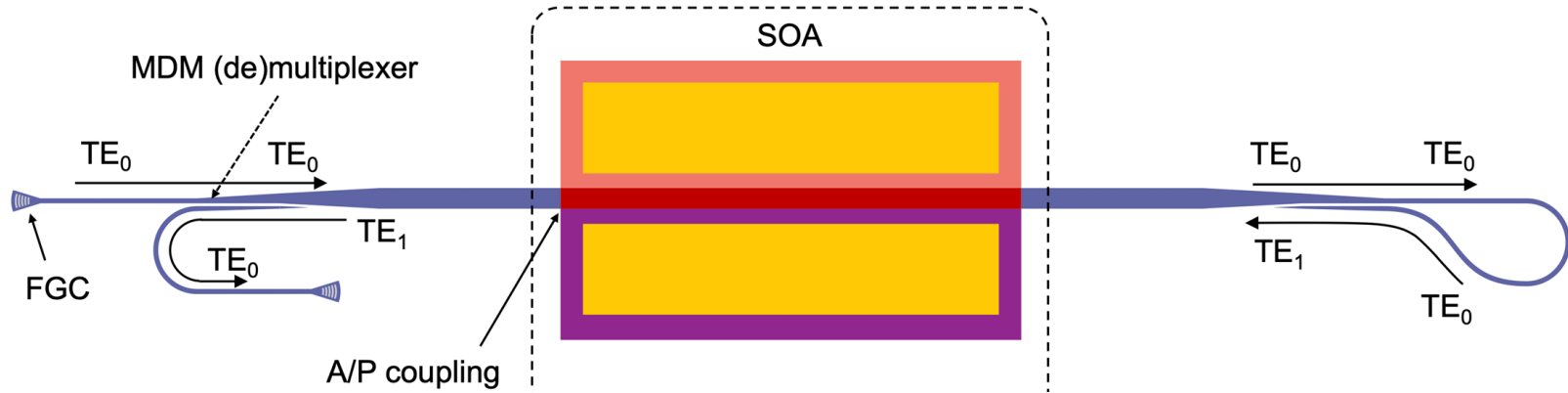
- Combining mode multiplexers and amplifiers made possible InP membrane technology
- TE_1 experiences slightly lower gain than TE_0



Boosting efficiency of SOAs

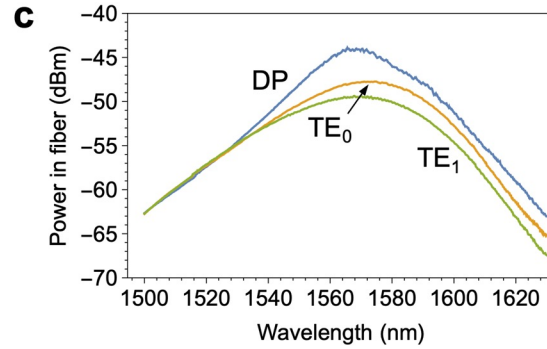
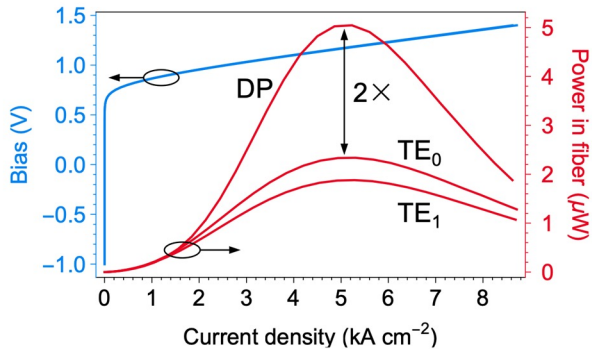
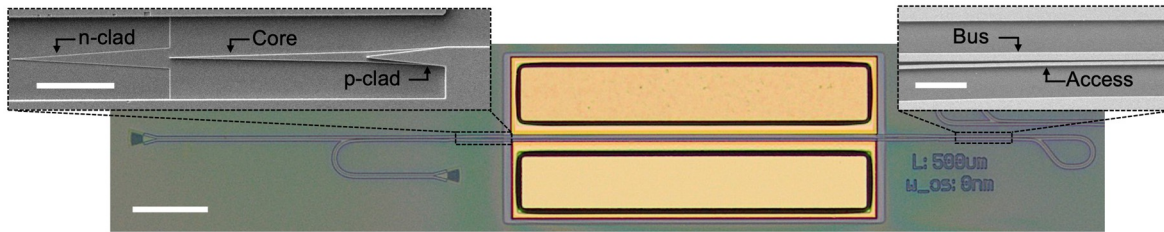
Non-resonant 2-pass SOAs based on mode multiplexing (patent pending):

- Low-crosstalk in the MDM coupler suppresses resonance;
- Gain boosted without increase in pump current, and/or
- “Halved” footprint and pumped energy for the same gain.



Boosting efficiency of SOAs

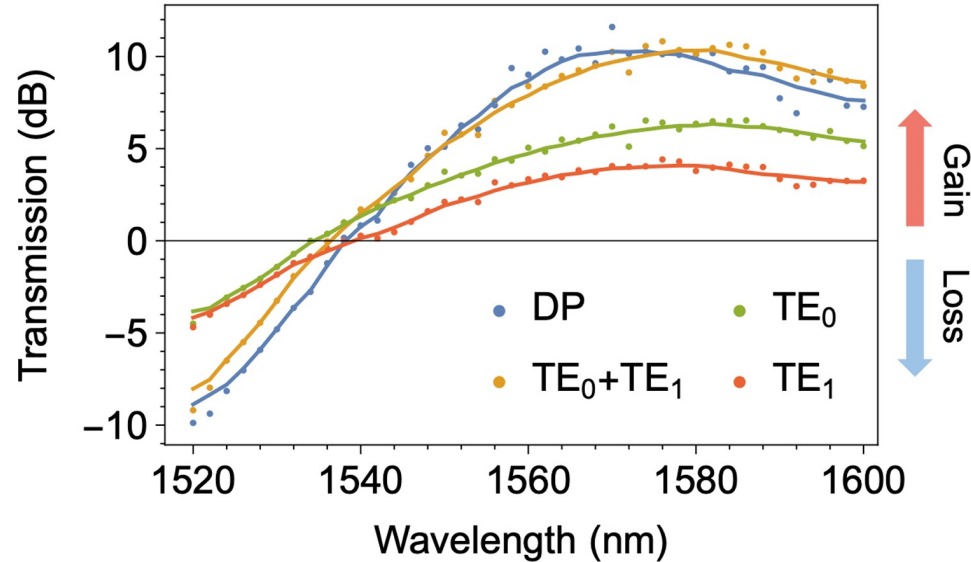
2-pass amplified spontaneous emission:



Boosting efficiency of SOAs

2-pass net modal gain (500um long SOA at 4.1 kA/cm²):

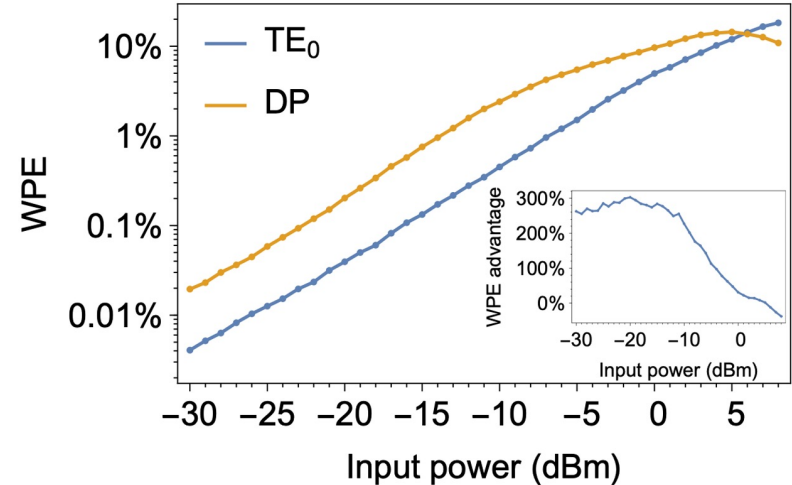
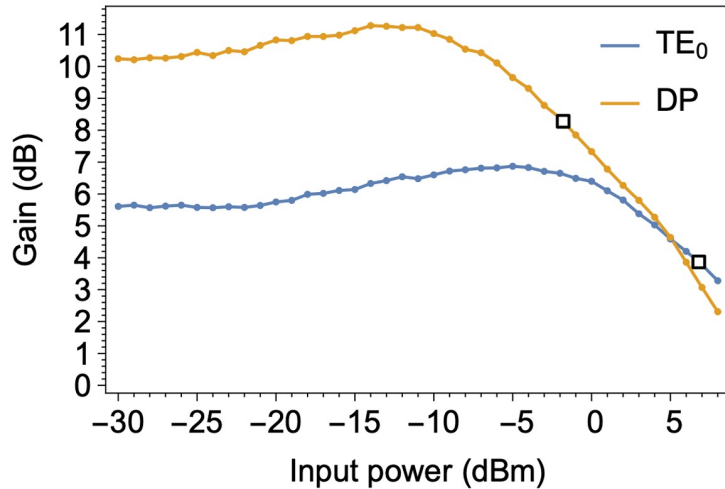
- Gain boosted from 6.2 dB for single pass to 11.6 dB (87% enhancement)
- Absorption (as EAM) also boosted as seen in 1520-1540nm region
- Universal circuit-level method applicable to any PIC platform



Boosting efficiency of SOAs

Saturation is earlier for 2-pass than 1-pass;

Significant advantage for low input powers (which is the case for most telecom, datacom and switching applications): Wall-plug efficiency (>300% enhancement)



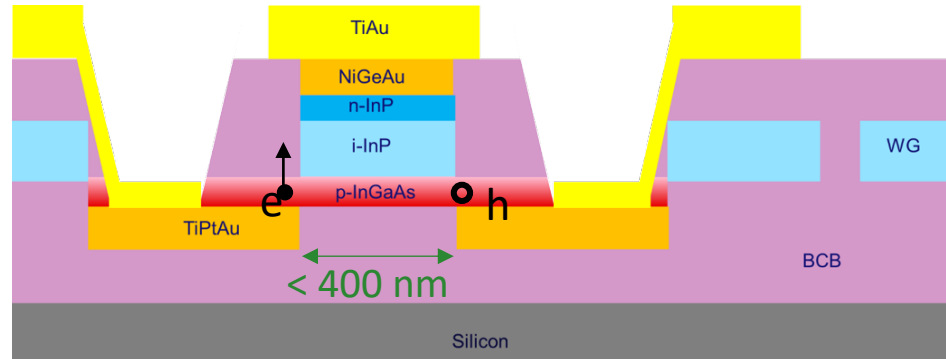
>110 GHz photodiode

Conventional design

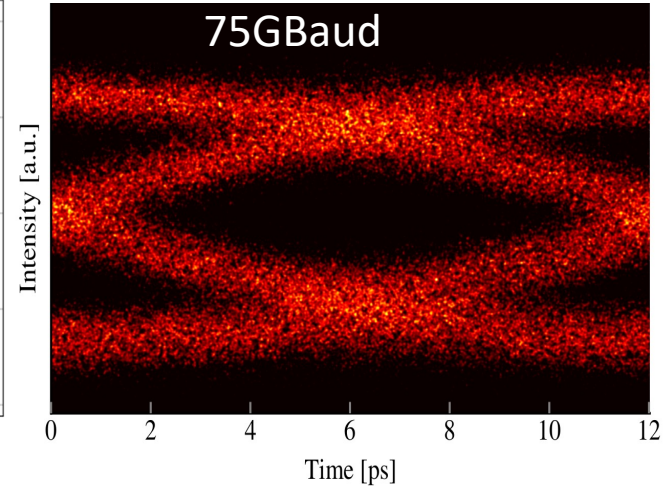
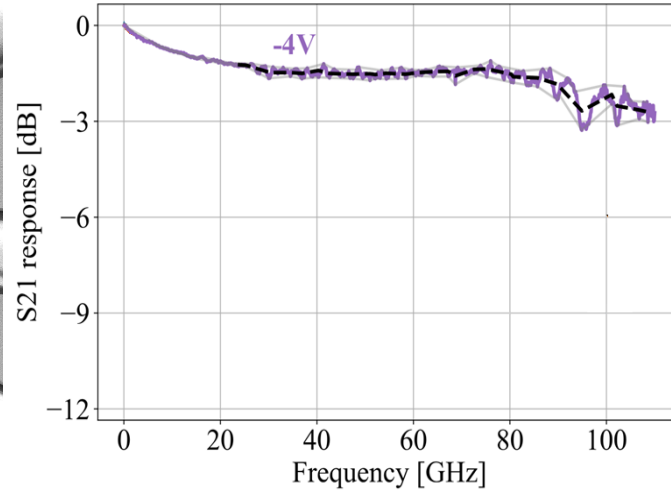
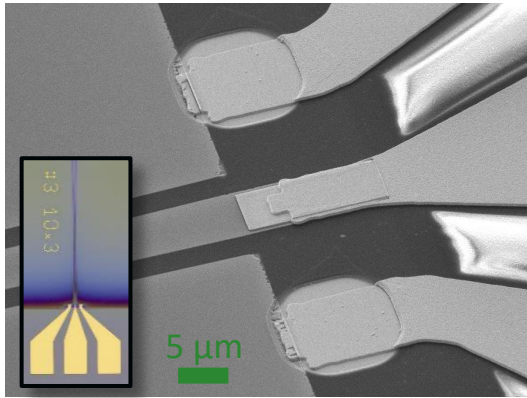


Our design

Closer metal contacts without
loss compromise



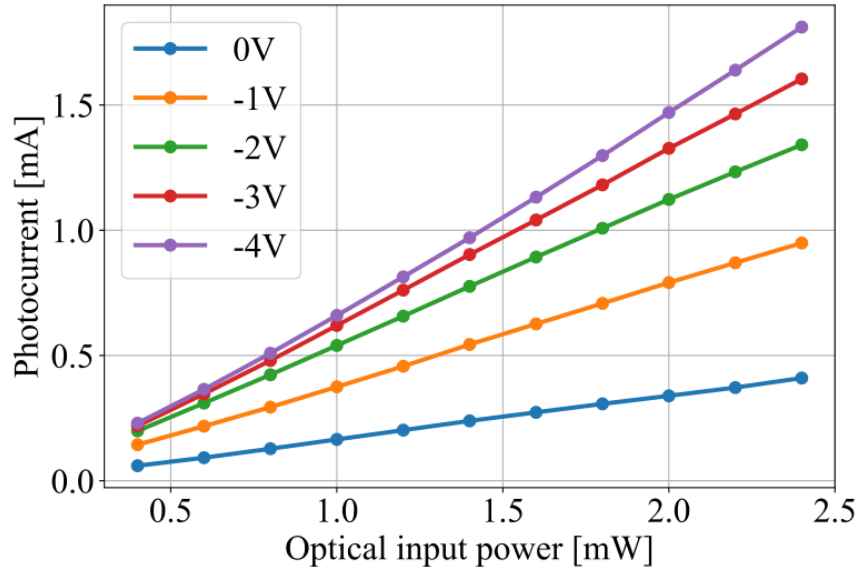
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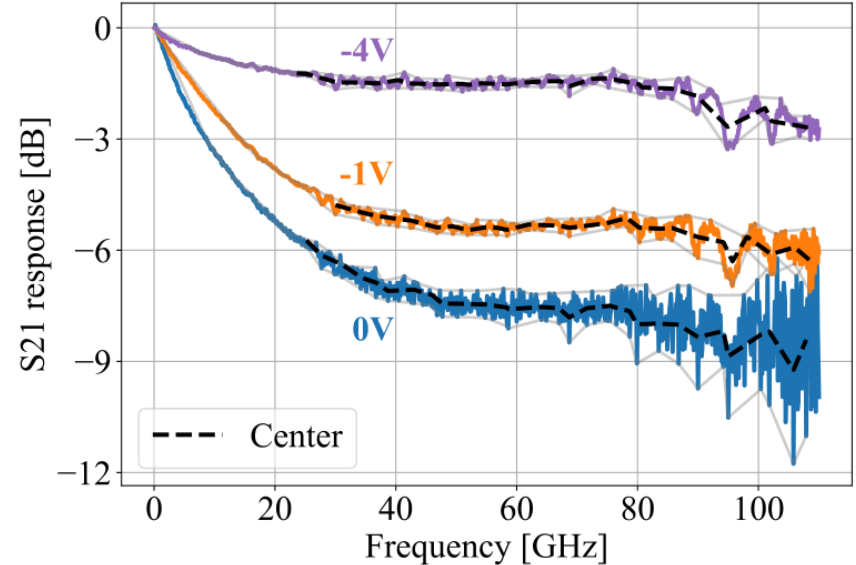
Micron-square footprint: 5 x 2 micron²

InP membrane platform for density and speed scaling

>110 GHz photodiode

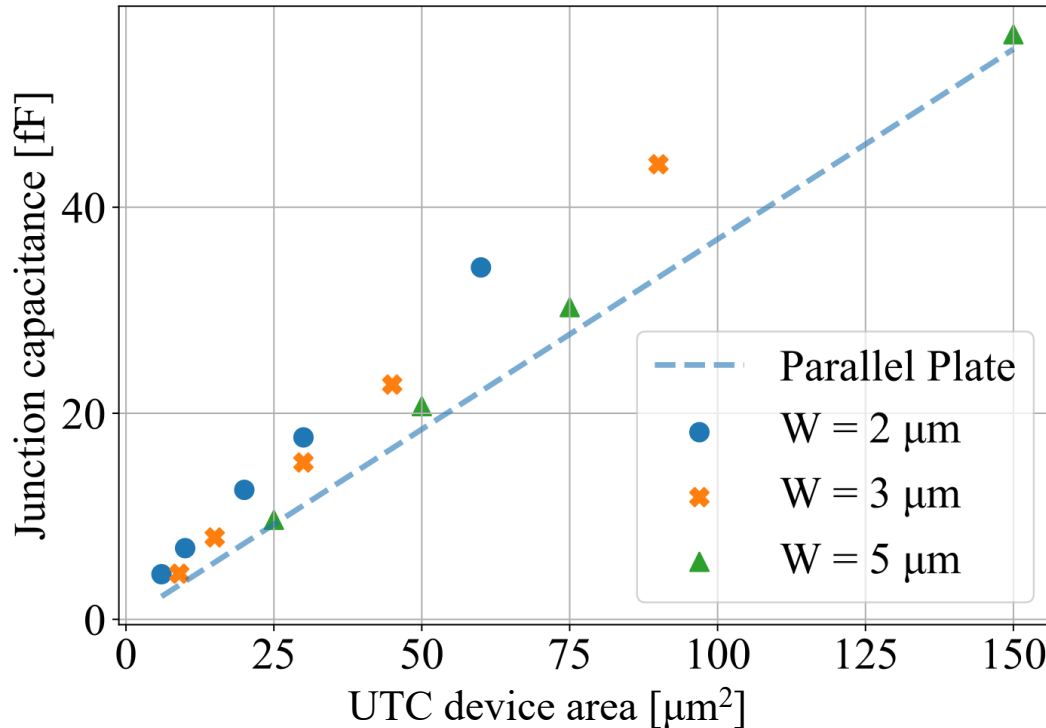


0.6 - 0.7 A/W responsivity
5 x 2 micron² photodiode area



No band-smoothing layers in this device;
resolved in a parallel work

Carrier diffusion limited design



Deviation from parallel plate model for 2 & 3 μm wide devices may be caused by a parasitic capacitance

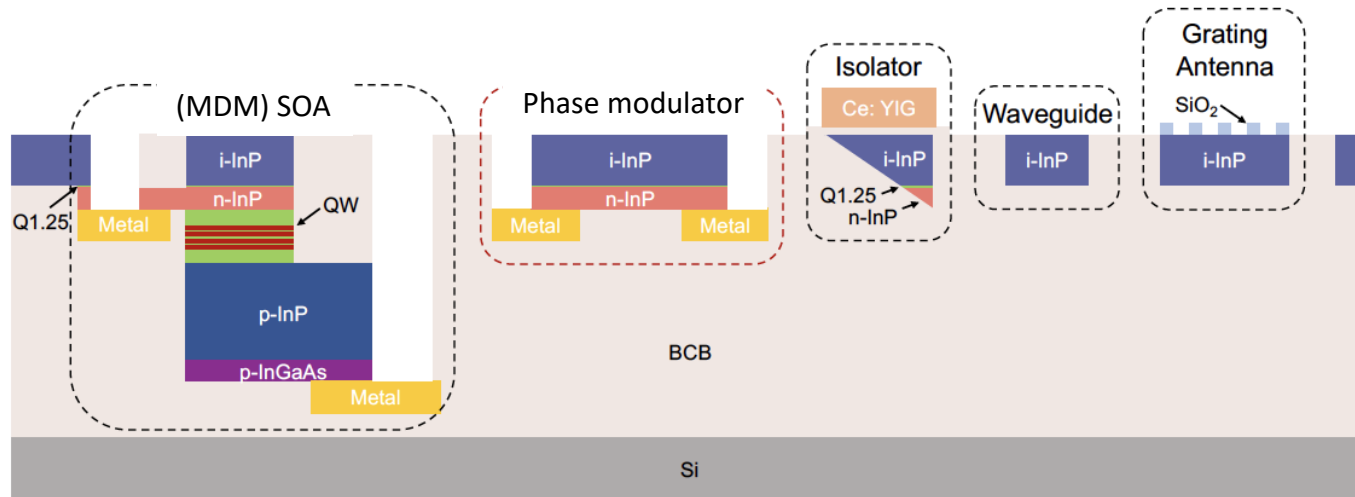
Leakage of the electric field around the edges of the structure.

Junction capacitance as low as 4.4 fF is achieved

Series resistance of the same device of 6.5 Ω

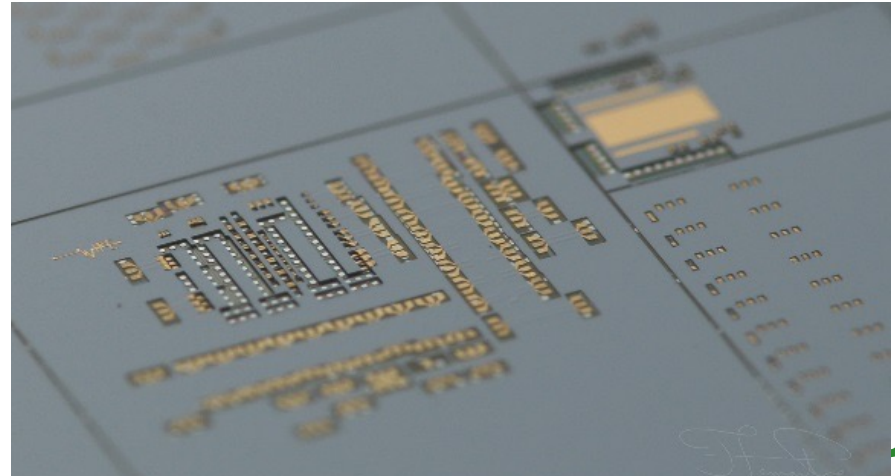
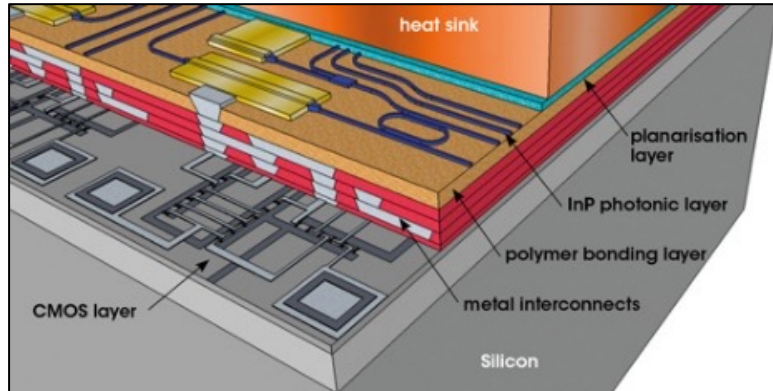
Laser and nanophotonics in one process flow

- An active-passive platform realized with a single process flow
- Eliminate the need of assembly or bonding for external light source



Wafer-scale assembly to electronics

- Full active-passive InP membrane (DFB, EAM, PD, etc) wafer bonded to a co-designed BiCMOS wafer
- High-density electrical vias eliminates the need to wire-bond or flip-chip
- For more details please attend Invited Talk Online, Yao et al, “Bringing photonics and electronics together for high-speed, high-density signaling”

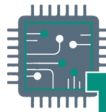


Summary

- Active-passive photonic integration on an InP membrane
- InP membrane nanophotonics enables compact and highly efficient Gain and EO devices
- Facilitates wafer-scale assembly to electronics



Gravitation



TWILIGHT

EU H2020



PHOTONICS PUBLIC PRIVATE PARTNERSHIP



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