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InP/GaAsSb DHBTs: THz Analog Performance and Record 180-Gb/s 5.5V_{ppd}-Swing PAM-4 DAC-Driver (Invited)

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***Abstract*—"Type-II" InP/GaAsSb DHBTs are the first non-GaInAs -based transistors to show oscillation frequencies > 1 THz with the associated benefits of higher breakdown voltages, low power dissipation, and superior linearity and scaling characteristics. Whereas no large-signal characterization of THz transistors is found in the literature, THz InP/GaAsSb DHBTs display attractive 94 GHz load-pull characteristics, and less aggressively scaled devices achieve record saturated output power and output power density per unit emitter area. The physical advantages of Type-II InP/GaAsSb are reviewed here. Beyond impressive analog small/large-signal performance metrics, we report a record mixed-signal performance for a PAM-4 DAC-driver designed and fabricated at III-V Lab in a 0.7-µm InP/GaAsSb DHBT technology implemented on epitaxial layers grown at ETHZ. The DAC-driver offers an unprecedented 5.5-Vppd 90-GBd (180 Gb/s) differential output swing with high eye diagram quality and over 12-dB gain control capability at a 1.1-W power consumption, leading to a record 3.1-GBd E/O modulator driver figure-of-merit (FoM). PAM-4 operation at 112-Gb (224 Gb/s) is also demonstrated with 3.35-Vppd and 0.6-W dissipation, also with a record 2.6-GBb E/O FoM. A 110 GHz bandwidth linear driver with a 16.7 dB gain and 0.85-W consumption was also implemented in the same technology, enabling a 4.1-Vppd output swing at 100 Gb/s both in PAM-4 and NRZ signaling. The all-around outstanding performance of InP/GaAsSb DHBTs makes them attractive for a wide variety of analog and mixed-signal circuit blocks used in modern telecommunication applications.**

Keywords—Type-II DHBTs, InP/GaAsSb, Power Amplifiers (PAs), Pulse-Amplitude Modulation Format (PAM-4), Linear Driver, Analog/Digital Circuits

I. Introduction

"Type-II" double heterojunction bipolar transistors (DHBTs) based on the InP-Ga(In)AsSb material system provide the highest available $f_T \times BV_{CEO}$ and $f_{MAX} \times BV_{CEO}$ products, as well as the highest reported f_{MAX} for a bipolar transistor [1]. Quaternary InP/GaInAsSb DHBTs also enabled the highest transistor f_T ever reported [2]. With a colleague from SFU, the first author secured a modest Canadian NSERC grant targeting the development of 150 GHz transistors in 1996 [3], and initiated InP/GaAsSb DHBT work with the epitaxy InP-GaAsSb heterostructures and the measurement of their band alignment [4]. With a remarkably fast "lab-to-fab" transition, GaAsSb-based DHBTs went into industrial production in 2004/5, following the transfer of a basic process from our Group to *HP Labs* (Palo Alto, CA) in 2001. Over the last 25 years, InP/GaAsSb DHBTs evolved from (75×75) µm^2 devices to the *first* non GaInAs-based transistors with $f_{MAX} > 1$ THz, and the *only* THz transistor to be organically developed, from DC to THz bandwidths, entirely within one group (first at SFU, and since 2006 at ETHZ). This unique development thread is even more surprising in that it was largely achieved by small teams of Ph.D. students and few postdoctoral fellows (pre-2008: 1 on epitaxy, 2 on device technology), with an infinitesimal fraction of the funding distributed by various agencies for THz technology — InP/GaAsSb DHBTs were perhaps *simply meant to be*. GaAsSb application to DHBTs now appears in the SRC 2020-2030 Decadal Plan [5], without reference to the field (though the Plan mentions "recent runs" show the resistance of GaAsSb to H_2 passivation in MOCVD-grown layers, a finding first reported in 1996 [6], and later confirmed in [7]). While on the topic of crediting prior art, it must be noted that the first InP/GaAsSb DHBTs were independently demonstrated by workers from *Rockwell* [6] and *Bellcore* [8] in 1996: initial results did not appear promising, and GaAsSb activities were promptly terminated. Interestingly, the *only* early industrial adopters of InP/GaAsSb technology (*Agilent*, and the defunct *Nortel*) *did not* have existing InP/GaInAs SHBT processes: they initiated InP/GaInAs and InP/GaAsSb DHBT development *in parallel*. Both organizations sped internal developments up by proofing their home-grown material with high-speed InP/GaAsSb DHBTs fabricated in the author`s group, before fabricating their own devices [9, 10]. It paid off: already with early insertion by the mid-2000`s, improved yields increased profits by $10k per T&M instrument sold by the former company [11].

In late 2021, the ETH-MWE Group demonstrated a new emitter fin process allowing the arbitrary tuning of the base access distance and yielding a record $f_{MAX} = 1.2$ THz in (0.25×4.4) µm^2 InP/GaAsSb DHBTs [1]. The devices offer an

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$f_{MAX} \times BV_{CEO} = 6.48$ THz-V, the highest ever reported in any transistor. A clear breakthrough in device scaling, 9.4-μm-long devices also achieve $f_{MAX} > 1$ THz with an emitter area of 1.645 μm^2. In comparison, the previous InP DHBT state-of-the-art reported $f_{MAX} = 1.15$ THz with $BV_{CEO} = 3.5$ V and a 0.26 μm^2 emitter area [12]. The scaling and breakdown advantages of InP/GaAsSb technology are obvious. Further perspective is gained by defining $f_{AVG} = (f_T \times f_{MAX})^{½}$ as a figure-of-merit of balanced performance. This leads to a record InP DHBT metric of $f_{AVG} \times BV_{CEO} > 4$ THz-V, approaching the 4.49 THz-V of 20-nm GaN HEMTs [13] (reaching 4.9 THz-V with a less stringent BV_{CEO} defined at $J_C = 10$ kA/cm^2). InP/GaAsSb DHBTs also compare well to the highest reported InP HEMT performance with $f_T/f_{MAX} = 0.61/1.5$ THz and $BV_{DS} = 3$ V, with a corresponding $f_{MAX} \times BV_{DS} = 4.5$ THz-V and $f_{AVG} \times BV_{DS} < 2.9$ THz-V [14]. Despite a long list of favorable device metrics, the InP/GaAsSb DHBT literature remains sparse in terms of their use in circuits (with few exceptions [15-16], including a record efficiency 0.5 THz oscillator [16]). We partly remedy this situation below with leading edge high-performance circuit demonstrations.

This paper is organized as follows: Section II outlines unique device operation advantages of InP/GaAsSb DHBTs. Section III shows properties of InP/GaAsSb DHBTs pertinent to analog power amplifiers (PAs) operating at mm- and sub-mm-wave frequencies. Section IV describes a 0.7-μm technology developed at III-V Lab on ETHZ epilayers, and its application to record-setting high-symbol-rate large-output-swing integrated circuits (ICs).

II. InP/GaAsSb Type-II DHBTs

A. Band Diagram and Device Operation

Fig. 1 shows the equilibrium band diagram of a graded-base InP/GaAsSb DHBT. A composite InP emitter with a graded GaInP layer results in $\Delta E_C = 0$ eV at the E/B junction: this favors thermal injection of electrons into the base and leads to a collector current ideality factor $n_C = 1.0$, increases gain and ensures the sharpest device turn-on while contributing to a low-power dissipation. Turn-on voltages are lower than in Silicon BJTs (because the GaAsSb energy gap is only ~0.72 eV).

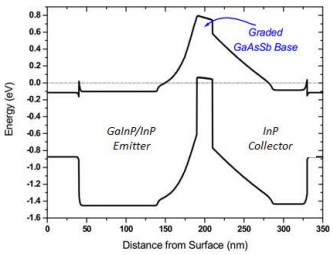

Fig. 1. Equilibrium band diagram of a graded-base InP/GaAsSb DHBT. The GaAsSb base uses compositional and C-doping gradings. Note the rather unusual mixed-group V grading, an innovation introduced by the ETH-MWE. Also note $\Delta E_C = 0$ eV at the E/B junction, and the large ΔE_V at both junctions.

The "Type-II" band alignment between InP and GaAsSb allows the use of an abrupt heterojunction at the base-collector interface with a binary InP collector. This inherently provides several advantages: InP shows high peak and saturated drift velocities for electrons, high breakdown fields, as well as a much higher thermal conductivity than GaInAs/AlInAs layers. The InP/GaAsSb band line-up allows electron collection in InP down $V_{CB} < 0$ V, permitting excellent device performance down to low V_{CE}, an advantage for low-power dissipation and large signal swing applications. Furthermore, InP enables selective wet etching of the collector and sub-collector layers during fabrication, a manufacturing advantage [11] at least as significant as GaInP emitters were for GaAs HBTs.

The sizable valence band discontinuity ΔE_V at the E/B and B/C junctions not only eliminates hole back-injection into the emitter, but it also suppresses the base pushout experienced in homojunction collectors at high collector current densities and low V_{CE}. To some extent, base pushout also takes place in InP/GaInAs DHBTs using a GaInAs spacer between the base and the collector grading layer. As pointed out by others [17], the base-pushout saturation charge storage degrades transistor performance in analog and mixed-signal applications which cause the B/C junction to become forward-biased (particularly in switching-mode PAs which drive bipolar transistors between cutoff and saturation [17], but also in conventional PAs and digital circuits). As shown in Section IV, InP/GaAsSb DHBTs indeed provide outstanding mixed-signal circuit performance.

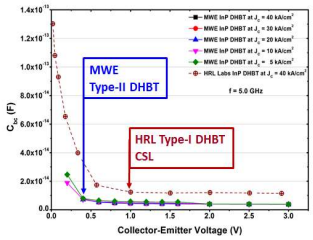

Fig. 2. C_{BC} variation at 5 GHz in InP/GaAsSb and InP/GaInAs with a CSL-graded collector for relatively low J_C. In contrast to GaInAs, the Type-II DHBTs show little variation untill $V_{CE} < 0.5$ V. GaInAs data from [18].

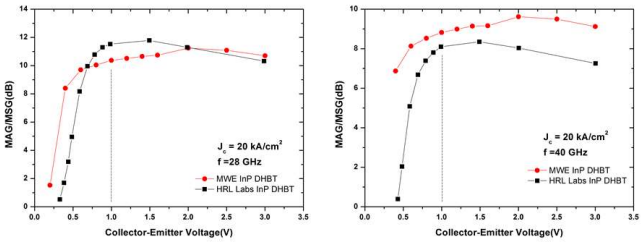

Fig. 3. Zampardi-style [18] 28/40 GHz RF knee measurements for the devices of Fig. 2. Type-II devices show better gain stability *vs.* V_{CE} (and hence overall RF linearity). The InP/GaAsSb DHBT advantage grows at higher frequencies.

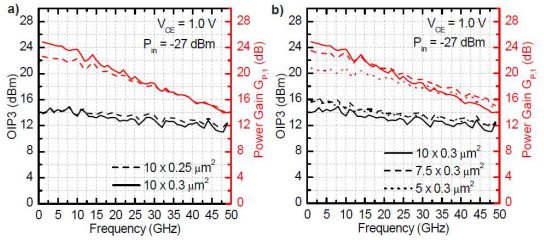

Fig. 4. (a) OIP3 and G_P of InP/GaAsSb DHBTs with (a) different emitter widths and (b) different emitter lengths as a function of center frequency. IMD measurements were taken with a 4 MHz tone spacing and a 50 Ω load. Devices were biased for best f_T/f_{MAX}. OIP3 degrades by 1-2 dB between 10 and 40 GHz.

High-current low-voltage effects in the collector region of bipolar transistors also lead to variations of the collector-base feedback capacitance C_{BC} —Zampardi *et al*. showed the C_{BC} variation at low V_{CE} is the major contributor to HBT nonlinearity [18]. One expects that a Type-I discontinuity in the B/C region exacerbates this effect when the bands flatten due to the electron space charge at high J_C and low V_{CE}, with the added complication of the previously discussed base pushout [14]. Indeed, UIUC workers first compared the linearity of InP/GaAsSb DHBTs and InP/GaInAs DHBTs with a chirped superlattice (CSL) collector, and found the former to offer better linearity at 18 GHz [19]. More recently, Bolognesi *et al.* reported the superior linearity of "Type-II" InP/GaAsSb DHBTs (with f_T/f_{MAX} = 480/640 GHz and BV_{CEO} = 5V) with respect to "Type-I" InP/GaInAs DHBTs, GaAs, and SiGe HBTs at low collector current levels [20]. Fig. 4 shows OIP3 and gain data *vs*. frequency for InP/GaAsSb DHBTs. OIP3 and G_P load-pull contours of InP/GaAsSb DHBTs show that the high linearity and gain domains overlap well in the Smith chart. The OIP3 *vs*. J_C curves of InP/GaAsSb DHBTs at 40 GHz show values similar to those of CSL-graded InP/GaInAs DHBTs (f_{MAX} = 650 GHz) measured at 10 GHz [21]. Recent ETHZ-MWE work to be reported elsewhere shows the linearity of InP/GaAsSb DHBTs is maintained at bias conditions needed for class-A and AB PA operation.

B. InP DHBT Collector Transport Comparison

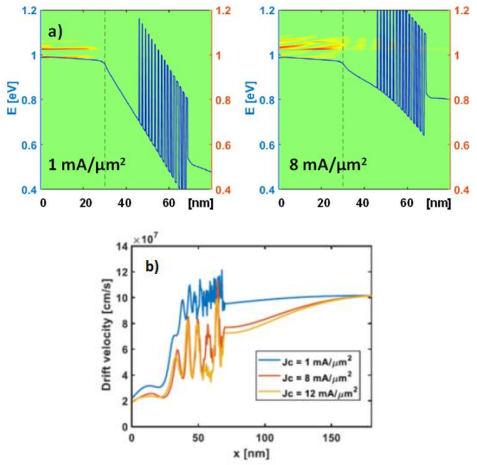

Fig. 5. Quantum-transport (QT) simulation of a chirp-superlattice graded InP/GaInAs DHBT. (a) band profile at low- and high-J_C: red indicates a high current density, green no current. (b) electron velocity profile.

Because transistor linearity is a key consideration for PAs and modulator drivers used with higher-order modulation formats in high-capacity modern telecom systems, it is worth examining the effect of collector structures on transport to understand how their respective limitations arise. The following results are based on a ballistic 1-D full-band, atomistic quantum transport (QT) solver [22]: whereas commercial TCAD tools (such as used in [19]) rely on classical drift-diffusion (DD) or hydrodynamic (HD) models, without precise descriptions of energy band structures (*i.e.* Γ, L, and X-valleys), transient, or quantum mechanical phenomena (*e.g.* tunnelling), the following simulations offer the most physical treatment of DHBT collector transport to date. First consider an InP/GaInAs DHBT with a CSL grading: Fig. 5a) shows the collector region band diagram for low and high collector current densities, while Fig. 5b) shows the corresponding computed electron velocity through the collector. It is clear that transport is severely perturbed at high-J_C due to tunnelling suppression. High-J_C charge storage effects are also evidenced by a reduced velocity in the base. This illustrates that graded interfaces that work well for some transistor bias are achievable, but that it is nearly impossible to realize a grading that performs well over a wide range of biases. In other words, for a given grading design (CSL or other), a bias exists for optimal transport. Large-signal operation however induces large current/voltage swings which result in non-optimal collector transport over significant portions of the swing. Fig. 6 provides a similar simulation for a "Type-II" InP/GaAsSb DHBT: high-current effects decrease performance by field-reversal at high-J_C, but the impact on collector velocity is far weaker: there is little perturbation of transport in the collector, and nearly none in the base. This accounts for the weaker C_{BC} modulation experienced in "Type-II" DHBTs at low V_{CE}, as well as their superior linearity.

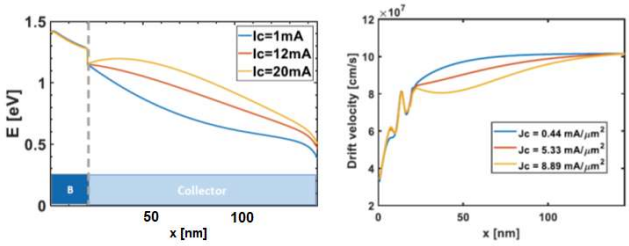

Fig. 6. (QT) simulation of an InP/GaAsSb DHBT: high-J_C conditions only marginally affect electron transport in the InP collector (right).

III. InP/GaAsSb DHBTs RF Properties

A. THz DHBT Small-Signal Performance

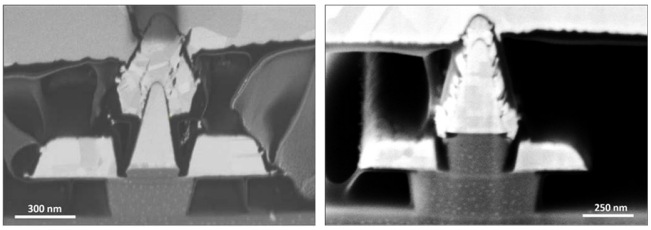

Fig. 7. Left: SEM image of an emitter fin InP/GaAsSb DHBT with a width of 250 nm and a 35 nm E/B access distance. The fin process allows much thinner semiconductor emitters compared to the standard process (right). From [1].

The recent ETHZ-MWE emitter-fin DHBT process enables: *i*) a tunable base-emitter access distance down to 10 nm, *ii*) the use of thick base contact metals (up to ~300 nm), and *iii*) the minimization of parasitic capacitances and resistances via precise lateral wet etching of the base-collector (B/C) mesa [1]. The process was demonstrated on a 20-nm $GaAs_xSb_{1-x}$ base, implemented with the As-mole fraction ramped from x = 0.59 at the emitter to x = 0.41 at the collector interface. The base layer also uses a linear grading of the carbon p-doping with an average level of 8.5×10^{19} cm^{-3}. The overall structure used a thinner 20 nm n+ InP emitter and 10 nm

GaInAs emitter contact layers to minimize the emitter undercut etching. For fabrication details, see [1]. Fig. 7 shows a cross-section of a typical device (left) *vs*. our standard process. The base contact resistivity is $\rho_{B,C} \approx 1\ \Omega\cdot\mu m^2$.

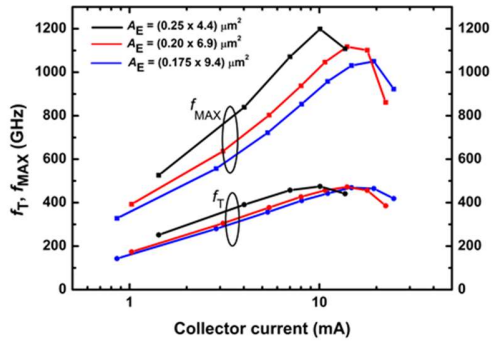

Fig. 8. Plot of f_T/f_{MAX} *vs*. collector current for various emitter mesa sizes with an E/B access distance of 35 nm. Several emitter sizes achieve $f_{MAX} > 1$ THz, including an emitter mesa length of 9.4 μm with $A_E = 1.645\ \mu m^2$ [1].

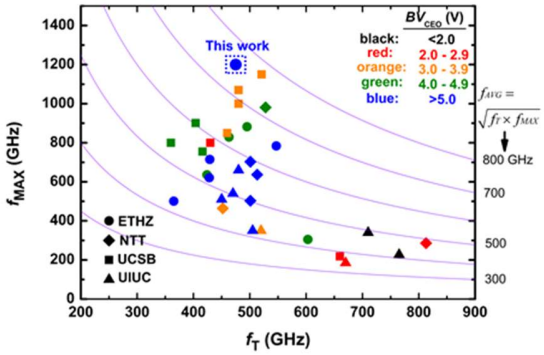

Fig. 9. Survey of reported InP DHBT metrics. Breakdown voltages are color-coded [1].

TABLE I
COMPARATIVE ASSESSMENT OF STATE-OF-THE-ART SiGe HBT, TYPE-I AND TYPE-II InP DHBTs

	SiGe HBT [34]	Type-I: GaInAs [12]	Type-II: GaAsSb [1]
Peak f_T (GHz)	505	520	475
Peak f_{MAX} (THz)	0.72	1.15	1.20
Emitter Area (μm^2)	8×(0.105×1.0)	0.13×2.0	0.25×4.4
BV_{CEO} (V)	1.6	3.5	5.4
$f_T \times BV_{CEO}$ (THz-V)	0.81	1.82	2.56
$f_{MAX} \times BV_{CEO}$ (THz-V)	1.15	4.03	6.48
V_{CE}/I_C (V/mA)	1.14 / 28.90	1.6 / 6.90	1.0 / 10.06
P_D/A_E (mW/μm^2)	42.31	42.46	9.15

Fig. 8 summarizes the measured RF performance for various device geometries. Thanks to the low base metal resistance contribution, devices with an emitter length of 9.4 μm achieve an unprecedented $f_{MAX} > 1$ THz—this is a clear breakthrough in THz DHBT scalability. Specifically, (0.20 × 6.9) μm² emitter devices show a peak $f_{MAX} = 1.10$ THz compared to 1.05 THz for (0.175 × 9.4) μm² DHBTs. As is usual with InP/GaAsSb DHBTs, high cutoff frequencies are accompanied by high BV_{CEO} values: Fig. 9 puts our results in perspective with other InP DHBT technologies with color-coded breakdown voltages. Table I contrasts record f_T/f_{MAX} HBTs from the literature. Type-II DHBTs offer significantly higher $f_{T,MAX} \times BV_{CEO}$ products. The dissipated power density in mW/μm^2 at the peak f_{MAX} bias point is also 4.6 times lower in InP/GaAsSb. Low power dissipation is advantageous in terms of efficiency, reduced self-heating and device reliability.

B. THz DHBT 94 GHz Large-Signal Performance

We performed single-tone continuous-wave CW power measurements at 94 GHz on single finger (0.175 × 9.4) μm² DHBTs biased for class-A operation. The source impedance was set to 50 Ω, and the load impedance was swept to determine the optimal load match for best saturation output power $P_{OUT,SAT}$ and power added efficiency (*PAE*). The best efficiency and saturated output power were obtained at $V_{CE} = 1.6$ and 1.9 V, respectively. These voltages are significantly higher than that yielding peak f_T/f_{MAX}. In all cases, the collector current density was ~8.5 mA/μm² at low-P_{in}.

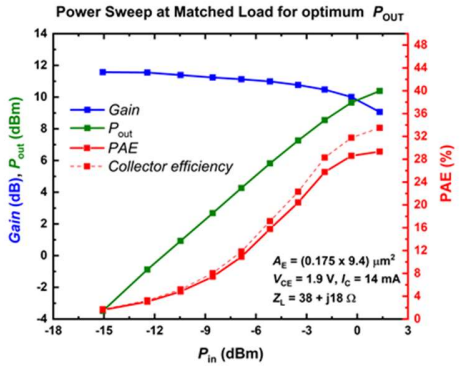

Fig. 10. 94 GHz single-tone CW power characteristics of a (0.175 × 9.4) μm^2 DHBT biased and matched for peak output power. [1].

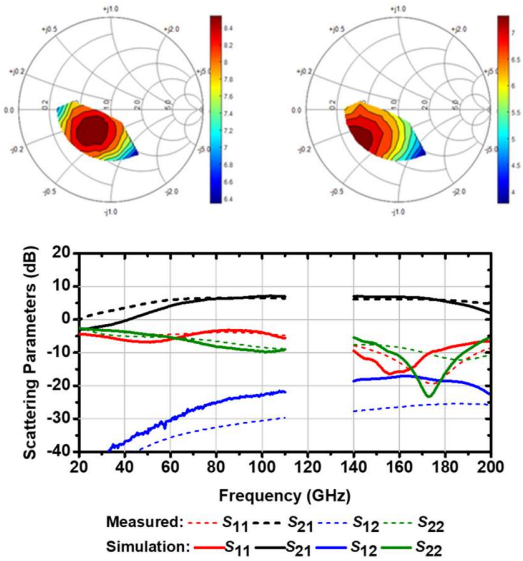

Fig. 11. 94 Top: GHz load-pull contours of a (0.3 × 9) μm² common-emitter single finger DHBT for optimum P_{OUT} (left) and optimum gain (right). Bottom: Ultra-wideband single-stage amplifier implemented with the same DHBTs.

When biased for efficiency an excellent *PAE* = 32.5% is obtained with simultaneous $P_{OUT,SAT} = 8.73$ dBm and a gain of 7.8 dB at 94 GHz. The collector efficiency is 40.3%, and the linear gain of the device at this bias is 11.85 dB. The peak

saturated output power at V_{CE} = 1.9 V and V_{BE} = 832 mV is 10.4 dBm with a corresponding gain of 9.1 dB and PAE = 29.3%, as shown in Fig. 10. This corresponds to a power density of 6.67 mW/μm^2 (1.17 W/mm). The optimum load impedances Z_L for peak efficiency and maximum output power are quite similar, indicating excellent device versatility. It is noteworthy that the V_{CE} biases used in these large-signal measurements far exceed the V_{CE} = 1.0 V required for peak small-signal performance: our 0.175 μm wide devices with peak f_{MAX} = 1.05 THz operate stably, with no evidence of degradation. Such device stability under aggressive large-signal operation suggests inherent reliability advantages in the InP-GaAsSb material system. No thermal management techniques (*e.g.* heatsinking or substrate thinning/transfer) were used: better performances can be expected with their application.

C. Sub-THz DHBT Large-Signal Performance at 94 GHz

The use of fine emitter widths to maximize f_{MAX} necessarily reduces the emitter area for a given emitter length: this limits the maximum deliverable output power per single emitter. For mm- and sub-mm-wave applications, the performance of wider emitter devices should also be investigated.

We characterized Type-II (0.3 × 9) μm^2 DHBTs realized in the standard (non-fin) ETHZ-MWE process. Load-pull measurements were carried out for single-finger common-emitter (0.3×9) μm^2 DHBTs in class-A bias. Contours for P_{OUT} at 3-dB-back-off input power are depicted in Fig. 11. The optimum load for maximum P_{OUT} is Z_L = (31.8 – j17) Ω. The domains of high output power extend close to the center of the Smith chart, and there is a good overlap with optimum gain impedances. As a demonstrator, a single-stage 60-160 GHz amplifier was fabricated. The small-signal RF amplifier gain is > 7 dB up to 110 GHz, and >7 dB to 160 GHz (Fig. 11, bottom). It delivers 8 dBm large-signal P_{OUT} at 94 GHz with a DC power consumption of only 34 mW. In other still unpublished work, a maximum saturation output power $P_{OUT,SAT}$ = 14.5 dBm and a 10.4 mW/μm^2 power density at 94 GHz were achieved for devices of similar size, a record for InP DHBTs measured at W-band (without thermal management techniques).

IV. From InP DHBT Technology to High-Symbol-Rate and Large-Output Swing Integrated Circuits

Advances in optical/electronic (O/E) technologies and in communication systems using new transmission formats allow higher transmission rates with increased spectral efficiency. Multi-level coded transmission, and in particular the four-level pulse-amplitude modulation (PAM-4) format, are widely used in optical communications. High-symbol-rate and large-swing drivers are key electronic components empowering modern high-capacity transmitters.

Indeed, to efficiently drive the electro-optical modulators that modulate the optical carrier, linear drivers must combine a wide output swing with a high gain-bandwidth product and a low power consumption. Such requirements are hence very demanding in terms of transistor performance: they must combine very high f_T/f_{MAX}, a wide safe operating area, and a high BV_{CEO}, while maintaining a high transconductance and performance stability under high thermal stress. InP/GaAsSb DHBTs provide a low turn-on voltage, a high current gain β, a low C_{BC}, and high cutoff frequencies with a high BV_{CE0} [1]: this combination makes them particularly interesting for very-high symbol-rate IC design.

A. InP/GaAsSb Epitaxy and III-V Lab 0.7-μm DHBT Process

Fig. 12. SEM microphotograph of a 0.7×5 μm² InP/GaAsSb DHBT.

The InP/GaAsSb DHBT structure was grown by metal organic vapor-phase epitaxy (MOVPE) on a 3-inch semi-insulating InP substrate at ETH-Zurich. The emitter cap layer includes a 5×10^{19}-cm^{-3} Si-doped In-rich InGaAs layer to minimize the emitter contact resistivity. Type-II DHBT emitter structure uses a composite 40-nm thick InP/GaInP emitter. A compositionally graded $GaAs_xSb_{1-x}$ base (with x = 0.6 on emitter side and x = 0.4 on collector side) reduces the base transit time. A base average C-doping of 8×10^{19} cm^{-3} keeps its sheet resistance low. The low-doped GaInP emitter reduces the Type-II ΔE_C at the E/B interface, and increases the current gain, as previously stated. The collector is a 130-nm-thick 2.5×10^{16}-cm^{-3} Si-doped InP layer, allowing a full collector depletion at low bias. The B/C layers resemble those of the THz DHBTs of Section III.A, illustrates the B/C design versatility.

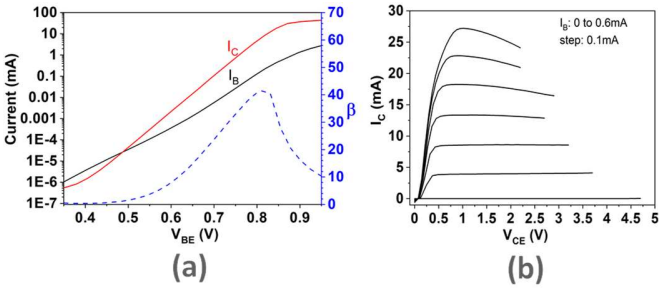

Fig. 13. 0.7×5 μm² InP/GaAsSb DHBT (a) Gummel plots at V_{BC}=0V and static current gain as a function of base-emitter voltage. (b) I_C-V_{CE} characteristics.

Type-II DHBTs were fabricated at III-V Lab using wet-etching and a self-aligned triple mesa technology. The process is similar to that commonly used to realize InP/GaInAs DHBTs [23]. Transistors have a hexagonal shape with a 0.7-μm emitter width and 5-, 7- and 10-μm emitter lengths. TLM measurements reveal an emitter contact resistivity of 4 Ω.μm^2, a base sheet resistance as low as 790 Ω/□, and a base contact resistivity of ~30 Ω.μm^2. The latter is 10× higher than obtained on GaInAs base of similar C-doping level at III-V Lab. As the Fermi level pins is closer to the valence band on GaAsSb than on GaInAs, further optimization of the base process is likely. Fig. 12 shows a scanning electron microscopy (SEM) view of the 0.7×5 μm² transistor before interconnect. Additional circuit

fabrication steps include NiCr thin film resistors, SiN MIM capacitors and three Au-based interconnection levels.

B. Device Performance

Gummel plots at a 0-V V_{BC}, and the DC gain, for a typical 0.7×5-μm² DHBT, are depicted in Fig. 13(a). The GaAsSb-based DHBT exhibits a peak DC gain of 42 at V_{BE} = 0.8 V. The base and collector ideality factors are 1.72 and 1.0, respectively.

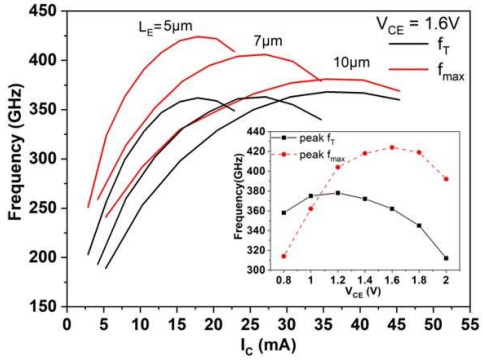

Fig. 14. f_T and f_{MAX} versus collector current for 0.7-μm InP/GaAsSb DHBTs with three different emitter lengths. The inset shows peak f_T and f_{MAX} as a function of emitter-collector voltage for a 0.7×5-μm² device.

Fig. 13(b) shows 0.7×5-μm² transistor output characteristics. 70-mV emitter-collector offset voltage is obtained as well as 0.5-V knee voltage, at a 6-mA/μm² collector current (J_C). The common emitter-collector breakdown voltage (BV_{CEO}) is 4.7 V at J_C = 30-μA/μm², with a large safe operating area. Transistor's negative output conductance, observed at high currents, indicates that self-heating occurs. The extracted thermal resistance at a 25-mW power (I_C = 15 mA and V_{CE} = 1.65 V) is 4.7 K/mW. Fig. 14 depicts f_T and f_{MAX} versus collector current for representative 0.7-μm devices, with different emitter lengths, at V_{CE} = 1.6 V. The peak f_T and f_{MAX} for 0.7×5-μm² DHBTs at J_C ~ 6 mA/μm² exceed 360 and 420 GHz, respectively. f_T slightly increases with emitter length whereas f_{MAX} decreases because the extrinsic base resistance does not scale inversely with emitter length. The Fig. 14 inset illustrates the peak frequency performance dependence on V_{CE} for a 0.7×5-μm² InP/GaAsSb DHBT, clearly showing higher f_T at lower V_{CE} (peak f_T ~ 380 GHz at V_{CE} = 1.2 V). The curves highlight the advantage of Type-II DHBTs in maintaining a high performance at low bias (V_{CE} < 1.2 V): in contrast to GaInAs-based DHBTs, no collector current blocking occurs when the B/C is slightly reverse biased. As shown below, this InP/GaAsSb DHBT technology is very well-suited to combined high symbol-rate and large output swing circuit applications.

C. InP/GaAsSb/InP-DHBT Lumped Linear Driver

1) Linear Driver Design

The lumped linear driver was designed and fabricated at III-V Lab around the 0.7-μm InP/GaAsSb DHBTs described in Section IV.A. A die microphotograph is shown in Fig. 15. The driver dimensions are 1.2×1.5 mm² and its active core region is 0.6×0.2 mm². The linear driver was designed using an electro-magnetic-circuit co-simulation design flow [24].

The driver has a three-stage differential-amplifying-cell architecture, and is composed of a pre-amplifier and a large-swing linear output stage. The pre-amplifier provides input impedance matching on a 100-Ω_{diff} source, differential gain, equalization capabilities and common-mode rejection to ensure good differential operation. Its amplifying cells consist of emitter followers and a resistively-degenerated differential pair to ensure linear operation. An additional emitter follower stage is interposed between the pre-amplifier and the output stage to ensure impedance matching and minimize bandwidth degradations. The output stage relies on a paralleled-transistor cascode differential architecture with emitter resistive degeneration [25], to combine a large linear output swing and a high gain-bandwidth product. Inductive peaking was implemented to further increase the driver equalization capabilities, as well as the overall bandwidth and the output impedance matching on a 100-Ω_{diff} load.

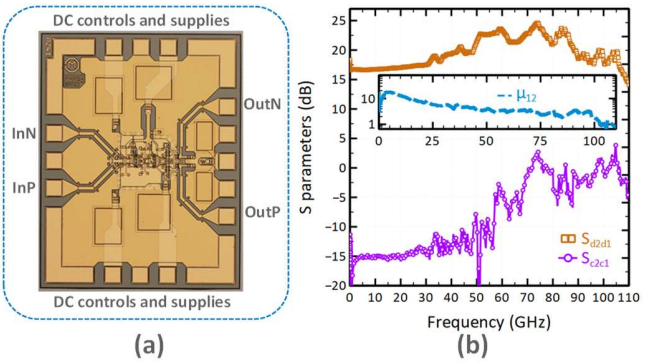

Fig. 15. InP/GaAsSb DHBT linear driver (a) die microphotograph. (b) Measured differential- and common-mode S-parameter gains. Inset: μ stability factor.

2) Linear Driver Characterisation and Performance

The linear driver S-parameter on-wafer measurements were conducted from 70 kHz to 110 GHz. Fig. 15(b), depicts the linear driver differential- and common-mode gains, as well as the μ stability factor, which have been retrieved from the single-ended S-parameter measurements (Fig. 15(b) inset). At 40 MHz, the differential gain, $|S_{d2d1}|$, is 16.7 dB, while the driver shows a beyond-110-GHz –3-dB-bandwidth, exceeding the vector network analyzer frequency range. This results in a gain-bandwidth product in excess of 752 GHz. This linear driver also shows high equalization capabilities with up to 7.9-dB of equalization gain at 74 GHz. Besides, as shown on Fig. 15(b), at low frequencies, a –15-dB common-mode gain, $|S_{c2c1}|$, is obtained, yielding a 31-dB common-mode rejection ratio (CMRR). The CMRR remains above 17 dB across 110 GHz, thus ensuring good differential operation across the entire driver bandwidth. Additionally, the lumped linear driver remains unconditionally stable up to 108 GHz (μ >1), thanks to a good impedance matching to the 100-Ω_{diff} source and load, and a low reverse gain (less than –30 dB across 110 GHz). Therefore, Type-II DHBTs offer some of the highest gain-bandwidth product and equalization capabilities when compared to the linear driver state-of-the-art, see [24-29].

Lumped linear driver on-wafer large-signal digital measurements were performed at 100 Gb/s, both with four-level pulse-amplitude modulation (PAM-4) and non-return-to-zero (NRZ) modulations. The Fig. 16(a) inset shows the (2^{15}–1)-bit 50-Gb/s PRBS input signals. Fig. 16(a) depicts the linear driver 4.1-Vppd 100-Gb/s NRZ output signal eye diagram with clear eye opening. This emphasizes the InP/GaAsSb-DHBT linear driver`s ability to combine a large-output swing with high-symbol-rate operation, while ensuring a high signal integrity. Indeed, a 3-V differential eye amplitude is obtained, while the eye signal-to-noise ratio (S/N) is 7 and the rms-jitter remains below 730 fs. To the best of the authors` knowledge, this constitutes the highest >3-Vppd 100-Gb/s NRZ eye S/N reported for a linear driver to date.

Fig. 16(b) shows the linear driver 4.1-Vppd 50-GBd PAM-4 output eye diagram with a driver power consumption of 0.85-W. The DAC input signals are depicted in the Fig. 16(b) inset, where strong setup limitations can be observed, thus limiting the driver output signal quality. During PAM-4 measurements, the DAC output stage currents were scaled to exceed the driver 1-dB compression point. Note that no digital signal processing (DSP) or post-processing were used in driver measurements. Additionally, a significant fraction of the driver equalization capabilities was absorbed to compensate for the setup bandwidth limitations.

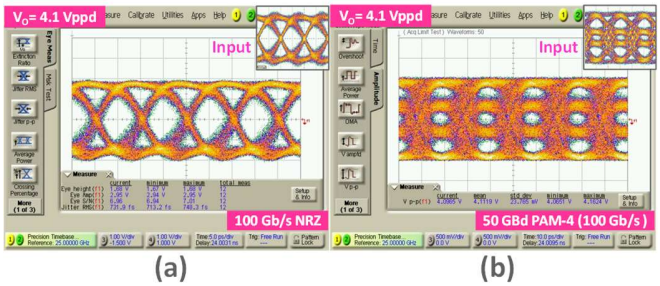

Fig. 16. InP/GaAsSb DHBT linear diver large-signal digital measurements (a) 100-Gb/s NRZ differential eye diagram. Horizontal and vertical scales are respectively 5 ps/div and 1 V/div. Inset: differential input signal. (b) 50-GBd PAM-4 differential eye diagram. Horizontal and vertical scales are respectively 10 ps/div and 1 V/div. Inset: differential input signal.

D. InP/GaAsSb/InP DHBT 2-bit DAC-Driver

One of the key architectures allowing for the combination of high-speed and high-swing is the power-DAC [30]. The power-DAC circuit was the basis of the first single-carrier 1.0 Tb/s transmitter [31].

The presented DAC-driver circuit [32] transforms 2 binary input data streams into an amplified PAM-4 differential output signal. This DAC-driver block diagram is shown in Fig. (a). Two NRZ input signals (LSB and MSB) are first converted from single-ended (SE) to differential ones (B1) and amplified (B2). The resulting signals are combined and amplified to obtain differential PAM-4 output signals. Specific control functionalities are also provided to optimize the E/O response of the combined driver and modulator. These functionalities are: output driving swing adjustment, static predistortion to compensate for the E/O characteristic nonlinearity, pre-compensating modulator's limited bandwidth and providing necessary DC offset.

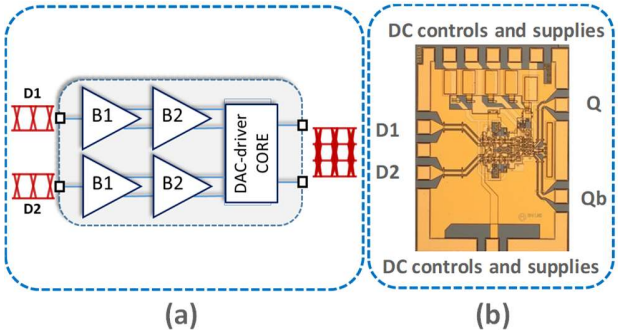

Fig. 17. InP/GaAsSb DHBT DAC-driver (a) circuit block diagram. (b) die microphotograph.

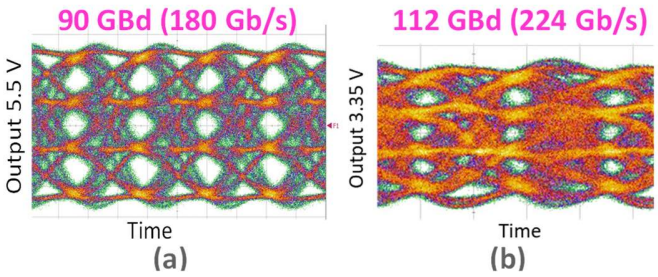

Fig. 18. InP/GaAsSb DHBT DAC-driver PAM-4 measurements. (a) 90-GBaud (180 Gb/s) PAM-4 5.5-Vppd output-swing differential eye diagram. Scale: (1V/div, 5ps/div). (b) 112-GBaud (224 Gb/s) PAM-4 3.35-Vppd output-swing differential eye diagram. Scale: (1V/div, 5ps/div).

Both electrical simulation and circuit layout obey high frequency design rules. A compact layout is privileged to maximally shorten signal interconnections. However, the output cascode block is a critical region, where thermal dissipation needs to be correctly addressed. The power density is high, and a proper trade-off between signal integrity and safe heat dissipation needs to be found.

The InP/GaAsSb DHBT IC shown in Fig. 17(b), was implemented in the III-V Lab 0.7-µm technology described in Section IV.A. It is composed of 37 transistors and its footprint is 1.2×1.5 mm², while the circuit's core dimensions are 520×470 µm². The DHBTs were operated at J_C = 5-6 mA/µm².

PAM-4 measurements of the DAC-driver at 90 GBd (180 Gb/s) and 112 GBd (224 Gb/s) are presented in Fig. 18. The power consumption is 1.1 and 0.6-W for the two respective symbol-rates. It should be noted that our measurements include cables, transitions, delay lines and DC blocks, all of which impact signal integrity. The 90-GBd PAM-4 differential output eye diagram with a record 5.5-Vppd swing and an excellent eye quality is presented in Fig. 18(a). A gain control capability of over 12-dB was also obtained. The circuit measurements at 112 GBd in PAM-4 is presented in Fig. 18(b), also with a record 3.35-Vppd output swing. It should be noted that the 112 Gb/s measurement input interface has a significant negative impact on the input signal quality. The E/O driver figure-of-merit (FoM) in terms of the PAM-4 symbol-rate D_S, the differential output swing V_{Opp}, the differential output matching impedance Z_0, and the circuit's DC power consumption P_{DC} is

$$FoM = D_S V_{Opp}^2 / 8 Z_0 P_{DC},$$

leading to record FoM values of 3.1 and 2.6 GBd at 180 and 224 Gb/s, respectively. They are to be compared to the E/O FoM of 0.13 GBd achieved in a 256 Gbs PAM-4 generator IC implemented around 0.25-µm InP/GaInAs DHBTs with f_T/f_{MAX} = 460/480 GHz (J_C = 10-13 mA/µm^2) [33]. Our data demonstrate the outstanding properties of InP/GaAsSb DHBTs for high symbol-rate large output swing mixed-signal ICs: a favorable band structure is key —raw transistor metrics (*i.e.* high peak f_T/f_{MAX} and J_C) are *not* sole determinants of mixed-signal IC performance. A high performance over wide signal swings is a strong advantage of "Type-II" DHBTs technology.

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