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InP DHBT on-wafer RF characterization and small-signal modelling up to 220 GHz

N. Davy[#*], M. Deng[*], V. Nodjiadjim[#], C. Mukherjee[*], M. Riet[#], C. Mismer[#], B. Ardouin[#], C. Maneux[*]

[#]III-V Lab, joint lab between Nokia, Thales and CEA Leti, 91767 Palaiseau, France

[*]IMS Laboratory, University of Bordeaux, CNRS UMR 5218, Bordeaux INP, Talence, France

nil.davy@3-5lab.fr

***Abstract* — In this paper, we perform on-wafer characterization of an InP double heterojunction bipolar (InP DHBT) up to 220 GHz using conventional characterization and de-embedding methods. Transistor measurements are analyzed through a comparison with the small-signal model simulation. Transistor accesses are modeled in order to understand how parasitic parameters are distributed and to propose subsequent improvements.**

***Keywords* — On-wafer characterization, Millimeter-wave, Double heterojunction bipolar transistor (DHBT), InP/InGaAs, Indium Phosphide (InP)**

I. INTRODUCTION

The world today is experiencing the era of intensive advancements in communications, as the amount of consumed data grows more and more with the emergence of new demands in the form of remote working or video streaming. Consequently, these new services have created a growing demand for high speed optical fiber systems [1] that will require even faster electronic systems.

Due to their high operating frequencies associated with high breakdown voltages, InP double heterojunction bipolar transistors (InP DHBTs) have a major role to play in communication value chain. Indeed, maximum oscillation frequency f_{MAX} higher than 1 THz has been reached with both type-I [2] and type-II [3] DHBTs while keeping a breakdown voltage BV_{CE0} higher than 4 V and 5 V, respectively.

As characterization up to THz frequencies are difficult and very expensive, InP DHBT RF figures of merit are commonly extrapolated from lower frequency (< 110 GHz) measurements. However, the fact remains unchanged that accurate characterization at higher frequencies are needed to confirm the cut-off frequencies as well as to extract and validate the associated device compact model, and thus enabling the design of sub-millimeter-wave integrated circuits. Some previous works have already demonstrated InP DHBT characterization beyond 300 GHz [4], [5] using less conventional methods such as on-wafer calibration. With the emergence of 220 GHz broadband vector network analyzer (VNA) [6], it is now being considered feasible to fully characterize a wafer up to 220 GHz. In this context, on-wafer characterizations of transistors have been performed up to 220 GHz using conventional measurement procedures (i.e. off-wafer calibration and open-short de-embedding). Some limitations of this approach have become apparent that are needed to be analyzed in order to achieve the objectives of on-wafer transistor characterization up to 220 GHz. The rest of this paper is organized as follows: section II details the technology under test and the RF test structure design. Section III details the measurements and the modelling of a single transistor. The parasitic effects stemming from transistor accesses are then studied and modelled followed by the conclusion.

II. TECHNOLOGY UNDER TEST

A. Technology description

The InP DHBT vertical structure is grown on a 3'' semi-insulated InP substrate using Solid Source Molecular Beam Epitaxy (SSMBE) by IntelliEpi. The intrinsic emitter is made of 40-nm thick InP Si- doped at 5×10^{17} cm^{-3}. The highly C-doped (8×10^{19} cm^{-3}) $In_xGa_{1-x}As$ base is 28-nm thick and is compositionally graded from x = 0.47 on the emitter side to x = 0.53 on the collector side in order to reduce the transit time. The 130-nm composite collector contains an unintentionally doped InGaAs spacer, a highly doped (4×10^{17} cm^{-3}) InP doping plane and a lightly doped InP collector ($< 2 \times 10^{16}$ cm^{-3}) to achieve a high breakdown voltage.

The transistors are fabricated using a wet-etch self-aligned triple mesa technology detailed in [7]. Various transistor geometries are available on this technology: the emitter width varies from 0.3-µm to 0.7-µm and the emitter length from 3-µm to 10-µm. Fig. 1 shows a scanning electron microscopy (SEM) view of a transistor before interconnections.

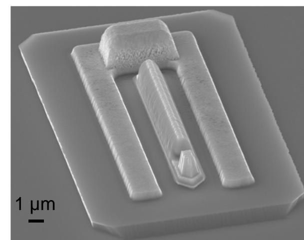

Fig. 1. Scanning electron microscopy of a 0.4 × 7 µm² InP DHBT

The performances of a 0.4 × 5 µm² InP DHBT has been detailed in [7]. The static current gain β is around 30 and the common emitter breakdown voltage BV_{CE0} is higher than 4.5 V. The frequency performances are $f_T = 380$ GHz and $f_{MAX} = 605$ GHz at $V_{CE} = 1.6$ V and $J_C = 5.8$ mA/µm².

B. *RF test structure design*

Transistor characterization up to 220 GHz requires the use of dedicated RF test structures. Fig. 2 shows the measured test structures. They have been optimized to achieve good measurement accuracy while maintaining a high density of transistors. These structures have demonstrated satisfying results up to 110 GHz as presented in [8].

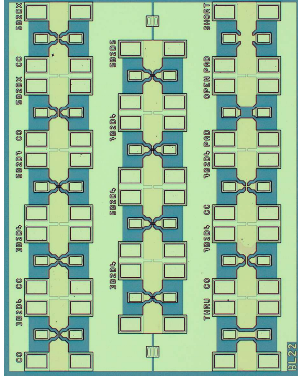

Fig. 2. Photograph of the measured RF test structures

A continuous ground plane that connects all test- structures together has been implemented following the recommendations of [4]. It allows to reduce both the probe-to-substrate coupling and the coupling between neighboring structures. The structures are arranged in a checkerboard configuration as introduced in [9]. Owing to this configuration, it is possible to reduce the distance between columns without increasing the coupling with other structures.

III. RESULTS AND DISCUSSION

Two sets of RF measurements were carried out to cover the 220 GHz spectrum. In the 1-110 GHz frequency range, measurements were performed with an Agilent E8361A VNA and a 100-µm pitch Picoprobe RF probes. In the 140-220 GHz range, measurements were performed using a Rohde and Schwartz ZVA 24 VNA with a ZC220 extender. The RF probes used in this band are 100-µm pitch Cascade Infinity probes. To ensure a good band continuity, the calibration method used in the two measurement bands is an off-wafer Short-Open-Load-Through (SOLT) calibration. It is performed using the ISS calibration kit GGB CS-5 in the lower band and the Cascade 138-357 in the upper band. The validity of this method has been proven up to 200 GHz [10].

A. *Transistor RF characterization*

The transistor under test has an emitter width of 0.4 µm and an emitter length of 7 µm. In order to remove parasitic effects due to the interconnects, an open-short de-embedding is applied. The transistor is biased at V_{CE} = 1.6 V as this bias point allows a good trade-off between the maximum values of f_T and f_{MAX}.

The transition (resp. maximum oscillation) frequency is then extracted with the current (resp. Mason's) gain-bandwidth product as shown in Fig. 3.

The extraction of the transition frequency f_T is quite straightforward as the current gain-bandwidth product is pretty flat for frequencies higher than 30 GHz. The extraction of the maximum oscillation frequency is, on the other hand, more complicated. In fact, two different values can be extracted for each bias point: a value between 25 and 60 GHz (values between 60 and 110 GHz are ignored due to the presence of probe signatures that strongly impact the gain bandwidth product) and another value between 140 and 200 GHz.

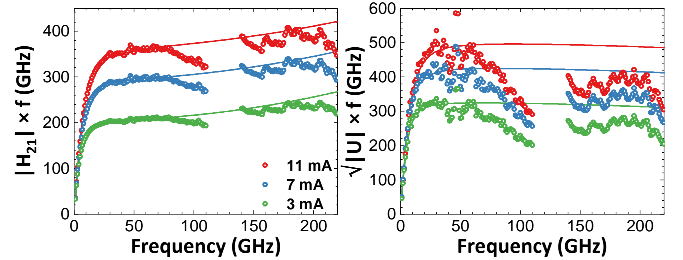

Fig. 3. Measurement (symbol) and small-signal model simulation (line) of current gain-bandwidth product (left) and Mason's gain-bandwidth product (right) at different collector current I_C and V_{CE} = 1.6 V

B. *Small-signal modelling*

In order to extract the value of the maximum oscillation frequency f_{MAX}, small-signal modelling of the transistor has been performed for different collector currents. Fig. 4 shows the chosen small-signal model.

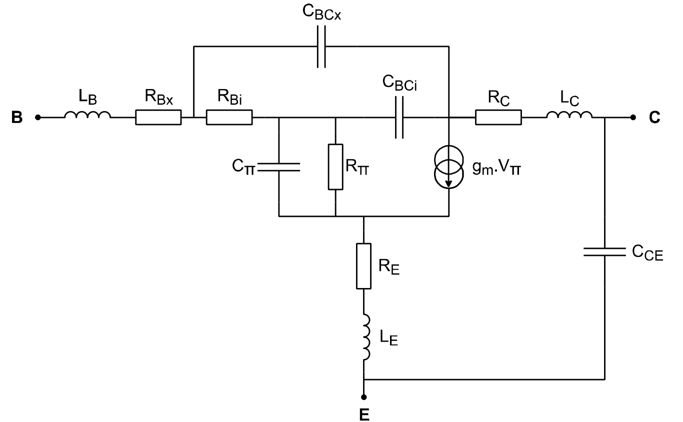

Fig. 4. Hybrid-π small-signal model of an InP DHBT

With the purpose of having a consistent modelling the model is split in two parts: the extrinsic part which is independent of the collector current and the intrinsic part which depends on it. Among the intrinsic elements, we use the following equations:

$$g_m = \frac{qI_C}{nkT} \tag{1}$$

$$R_\pi = \frac{\beta}{g_m} \tag{2}$$

$$C_\pi = C_{BE} + g_m\tau_F \tag{3}$$

with n being the ideality coefficient of the base-emitter junction and τ_F being the transit time.

Table 1 summarizes both the extrinsic and intrinsic small-signal parameters. The estimation of the intrinsic parameters requires the extraction of τ_F, β, R_{Bi}, R_{BC}, C_{BCi} at each bias point.

Extracted parameters behave as expected: R_{Bi} and C_{BCi} values decrease with the current. Moreover the value of the emitter resistance R_E, the collector resistance R_C, the extrinsic base-collector capacitance C_{BCx}, and the base-emitter capacitance C_{BE} are really close to their theoretical values [11]: $R_{E, th} = 3.3\ \Omega$, $R_{C, th} = 1.6\ \Omega$, $C_{BCx, th} = 6.2$ fF, and $C_{BE, th} = 19$ fF.

Table 1. Small-signal parameter values

Extrinsic parameters					
R_{Bx}	4.8 Ω	L_B	8.4 pH	C_{BCx}	6.6 fF
R_E	3.4 Ω	L_E	1.7 pH	C_{CE}	5.3 fF
R_C	2 Ω	L_C	8.1 pH	C_{BE}	17.5 fF

Intrinsic parameters			
I_C	**3 mA**	**7 mA**	**11 mA**
C_π	46.5 fF	79 fF	101 fF
R_π	444 Ω	203 Ω	140 Ω
g_m	75 mS	175 mS	275 mS
C_{BCi}	2.1 fF	1.6 fF	1.4 fF
R_{Bi}	16.2 Ω	13.5 Ω	12 Ω
R_{BC}	159 kΩ	105 kΩ	73 kΩ

The comparison between the measured and simulated S-parameters is plotted in Fig. 5 and Fig. 6. A good agreement between simulation and measurement results is obtained for most parameters. A slight discontinuity is observed among the two frequency bands. This is attributed to the signature of the probes and their positioning on the contact pads, considering the off-wafer SOLT probe-tip calibration. It is necessary to note, however, that an important difference is observed in the magnitude of S_{11} which could explain the behavior of the f_{MAX} gain-bandwidth product.

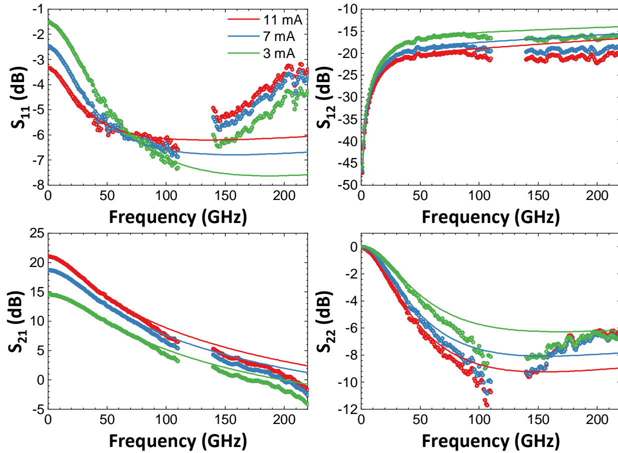

Fig. 5. Measured (symbol) and modelled (line) S-parameters' magnitude of a 0.4 × 7 µm² InP DHBT at different I_C

Gain-bandwidth products obtained from the simulations have been compared with the measured ones in Fig. 3. A good agreement is obtained for the current gain-bandwidth product on the two frequency bands. Regarding the Mason's gain bandwidth product, differences are observed from 60 GHz onwards. As explained before, the probe signature disrupts the measurements between 60 and 110 GHz. For the upper frequency band, the differences observed between the simulated and measured S-parameters is reflected on the f_{MAX} extraction. A detailed study of the steps preceding the extraction of the gain-bandwidth product could thus explain the inaccuracy in the upper frequency band.

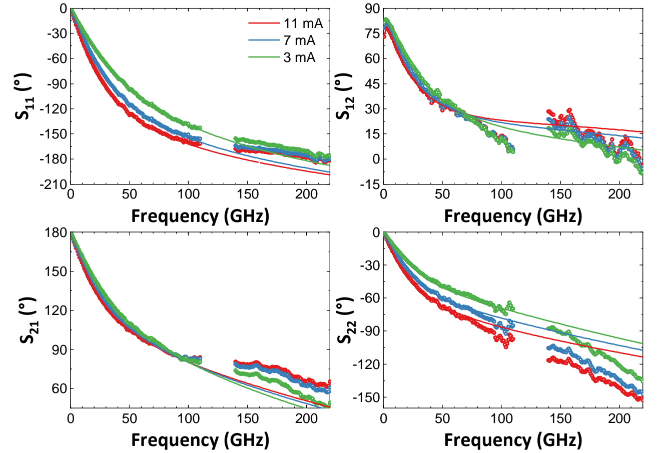

Fig. 6. Measured (symbol) and modelled (line) S-parameters' phase of a 0.4 × 7 µm² InP DHBT at different I_C

C. *Transistor access modelling*

Measurements presented in the previous section were processed using open-short de-embedding. For this de-embedding to be valid, open parallel parasitic and short series parasitic values must be constant over the whole frequency range. Fig. 7 shows the equivalent electrical circuit model of the open and short structures as well as the extracted inductances and capacitances. Both capacitance and inductance values are not constant in the upper frequency range which indicates that open short de-embedding is particularly not suitable in the *G*-band (140-220 GHz).

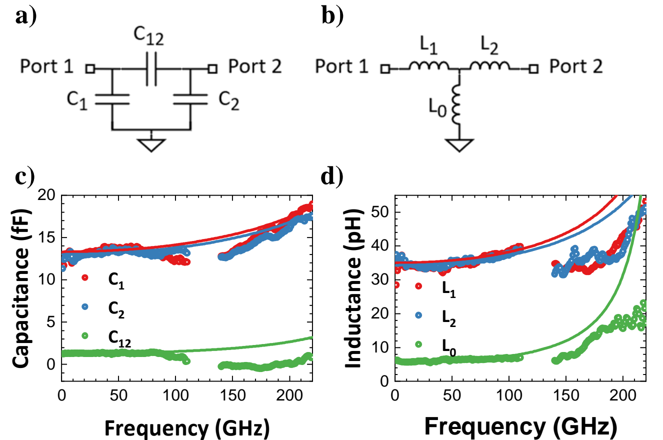

Fig. 7. Electrical equivalent model of the a) open b) short and extracted values of c) open capacitances and d) short inductances

More specifically, it indicates that parasitic elements are distributed and thus invalidates the model represented in Fig. 7. In order to understand the actual distribution of parasitics, the transistor accesses have been modelled. First, the pad is modelled using measurements of the pad-open and pad-short structures. Then, the full access is modelled using measurements of open and short structures. The equivalent electrical model of the open and the short structures as well as

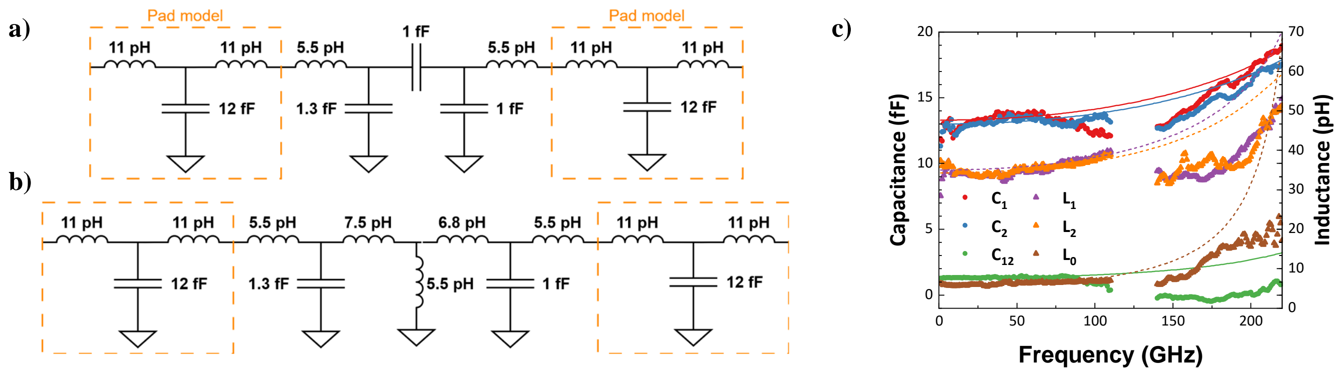

Fig. 8. a) Open equivalent electrical model b) Short equivalent electrical model c) Comparison between measurements (symbol) and model (line)

the comparison between measurements and model simulations are shown in Fig. 8.

Overall, a good agreement is obtained as depicted in Fig. 8(c).The four test-structures that are used for the modelling are shown in Fig. 9. The use of different probe designs, as well as a different placement of the probes, leads to discrepancies in the upper frequency range, particularly a shift of inductance values. Similarly, the C_{12} capacitance behaviour is strongly impacted by the probe design.

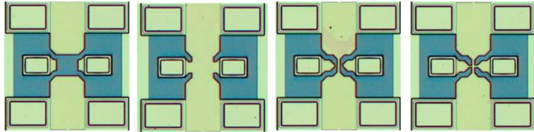

Fig. 9. Passives structures (left to right): pad-open, pad-short, open, short

Several insights emerge from the analysis of the equivalent electrical circuit model. As expected, parasitic elements are distributed. The pad itself features a distributed model and it contributes to more than 90% of the overall parasitic capacitances and around 50% of the inductances. The pad dimensions have already been reduced to the minimum allowed dimensions for probing. So, one way to further reduce the de-embedding parasitics would be to move the measurement reference plane closer to the DUT after calibration, so that the pad parasitics would be a part of the calibration step [12].

IV. Conclusion

We demonstrated the on-wafer RF measurements of an InP DHBT using conventional method such as off-wafer calibration and open-short de-embedding up to 220 GHz. In addition, we present a methodology to analyze the limitations that arise from this method. Small-signal modeling at multiple bias points allowed validation of the measurements up to 110 GHz. Furthermore, detailed study and modeling of the transistors accesses highlighted the distributed nature of parasitic elements in the *G*-band.

The detailed analysis presented in this paper opens up the way for 220 GHz broadband measurements. In particular, it highlights the fact that the use of an on-wafer calibration would be judicious to shift the reference plane of the measurements closer to the device. Thus, the conventional open-short de-embedding would still be valid in high frequency ranges.

Acknowledgment

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