

Electronics Letters

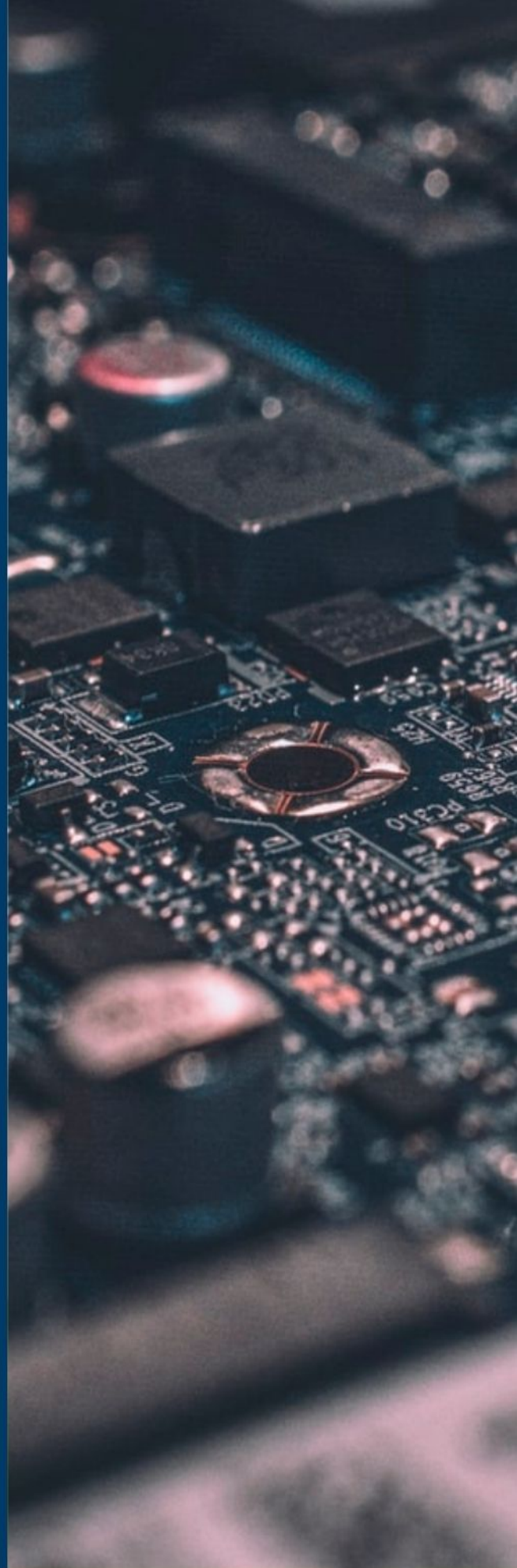
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106-GHz bandwidth InP DHBT linear driver with a $3\text{-}V_{\text{ppdiff}}$ swing at 80 GBd in PAM-4

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This Letter reports the design, fabrication and characterisation of a new differential linear driver, fabricated in the III-V Lab 0.7- μm emitter width indium phosphide (InP) double heterojunction bipolar transistor (DHBT) technology. Large-signal electrical characterisation shows 80-GBd symbol-rate four-level pulse amplitude (PAM-4) modulation conjugated with a driver output swing of $3\text{-}V_{\text{ppdiff}}$ and a 0.74-W power consumption. Thus resulting in a 1.22-GBd driving efficiency, the highest in over 70-GBd drivers' state-of-the-art, at that date. Accordingly, S-parameter measurements of the standalone linear driver exhibit the highest gain-bandwidth product of 556 GHz, in that current state-of-the-art.

Introduction: Hyperbolic global IP traffic growth together with 5G upcoming challenges are calling for an ever increasing transmission capacity in digital coherent systems of the core optical networks. To cope with that unprecedented demand, telecommunication vendors have been relying on spectrally efficient multi-level modulation format, such as PAM-4 and m-ary quadrature amplitude modulations (m-QAMs), generated by high-speed digital to analogue converters (DACs). In that context, the generation of four-level pulse amplitude modulation (PAM-4) electrical signals with an over 64 GBd symbol-rate is of prime interest.

Yet, state-of-the-art electro-optical (E/O) Mach-Zehnder modulator (MZM) face a drastic E/O bandwidth/required driving voltage trade-off [1]. In [2], the MZM yet reaches a 53.3-GHz V^{-1} figure-of-merit. Hence, differential linear drivers providing higher than 2 to $3 V_{\text{pp}}$ of linear output swing, as well as an over 100-GHz bandwidth and a low power consumption, are required for very high speed, energy efficient optical transmissions. Maximising the figure-of-merit defined by (1), that emphasises analogue front-ends' driving efficiency at a given symbol rate, is thus of prior importance

$$\text{FoM} = \frac{D_s \cdot V_{\text{Opp}}^2}{8 \cdot Z_0 \cdot P_{\text{DC}}} \quad (1)$$

where D_s is the PAM-4 symbol-rate, V_{Opp} is the single-ended or differential output swing at D_s , Z_0 is single-ended or differential output impedance matching and P_{DC} is the DC power consumption of the circuit.

III-V compound semiconductor-based transistors can provide very high cut-off frequencies (> 400 GHz) while ensuring high breakdown voltages (> 4 V) to switch high powers at very high speed, as shown in [3]. Therefore, being perfect candidates for these applications. Few works have shown over 64 GBd symbol-rate PAM-4 (or 16-QAM) generation, with an over $1\text{-}V_{\text{pp}}$ amplitude, up to date. Although some silicon- or silicon-germanium-based circuits show over 90-GHz bandwidth, as in [4, 5], published symbol-rate do not exceed 56 GBd. In [2], a 168-GBd polarisation division multiplexed (PDM) 16-QAM transmission is shown, multiplexing signals from four DACs, using two 0.25- μm InP DHBTs based 2 to 1 analogue multiplexer-driver, while both provides a $1.5\text{-}V_{\text{ppdiff}}$ output swing, a 110-GHz bandwidth, an about 8-dB peaking gain at 85 GHz and a power consumption of 0.99 W power consumption. Yet, power and latency hungry digital signal processing is here required. The authors of [6] report a very high-speed power DAC, based on a 0.7- μm width InP DHBT technology, which can generate 107 GBd PAM-4 signals with a $3.7\text{-}V_{\text{ppdiff}}$ output swing at a 2.9-W power consumption. Then, in [7], a commercially available differential linear InP amplifier shows 90-GBd PAM-4 signals with a $3.2\text{-}V_{\text{ppdiff}}$ output swing, a 55-GHz bandwidth and a power consumption of 3.6 W. However, neither of them conjugates the required output swing, bandwidth and power consumption to efficiently built an over 100-GHz E/O bandwidth transmitter.

In this Letter, we present a 106-GHz -3-dB bandwidth differential linear driver, fabricated in the III-V Lab 0.7- μm emitter width InP DHBT technology, with a PAM-4 linear output swing of $3\text{-}V_{\text{ppdiff}}$ at 80 GBd (160 Gb/s), together with a 0.74-W power consumption. Among those, 0.45 W are spent in the output driver. Circuit design and characterisation set-up are here described, as well as S-parameter, linearity and large swing high symbol-rate measurement results.

Design and architecture: The InP linear driver die is depicted in Fig. 1. It measures $1.2 \times 1.5 \text{ mm}^2$ while circuit core dimensions are $0.6 \times 0.2 \text{ mm}^2$. The driver is fully differential and composed of three amplifying cells, each relying on an emitter-follower and (cascode) differential pair cascade, based on the inter-gain-cells impedance mismatching principle. EM-circuit co-simulation, based on an ADS-momentum coupling, has been intensively used to obtain an accurate model of the circuit's behaviour, thus preventing bandwidth limitations and unstable operations that could come from inter-stage transmission lines and parasitic EM-couplings. Hence, all passive parts of the circuit have first been EM-simulated, then co-simulation was performed using the 0.7- μm InP DHBT thermo-electrical model. Series-feedback, through emitter resistive degeneration of all differential pairs in the circuit, has been implemented to improve both circuit's impedance matching and bandwidth, as well as to increase its linear dynamic. The driver input stage provides broadband input impedance matching and common-mode rejection to improve the circuit bandwidth and stability. To increase the signal-to-noise ratio, it features a 5-dB differential gain. The last preamplifier cell is further decreasing the common-mode gain while highly improving the impedance matching between the input amplifier and the output driver, which has a large capacitive input impedance. It thus improves the bandwidth at the expense of extra power consumption. Then, the output driver provides a 10-dB differential gain, together with 6.2 dB of peaking gain, through inductive peaking, that improves the bandwidth and the output impedance matching on a $100\text{-}\Omega_{\text{diff}}$ load. It also aims at compensating the E/O modulator bandwidth limitations. Moreover, a paralleled-transistor configuration has been implemented to both increase the linear output dynamic and to decrease transistor's thermal operating point, at the expense of input and output matching, caused by transistor's input and output capacitance summation. Therefore, to mitigate those effects, a cascode configuration has been used, improving the gain-bandwidth product and the input/output impedance matching, in minimising the Miller effects.

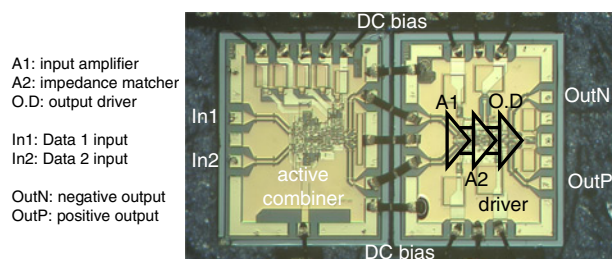


Fig. 1 In-house InP active combiner (on the left) and linear differential driver (on the right) assembly micro-photograph

InP DHBT technology: The III-V Lab in-house 0.7- μm InP DHBT technology, that served to fabricate this linear driver and the in-house active combiner depicted in Fig. 1, features, respectively, a 370 and 430-GHz f_T and f_{MAX} , an about 4-V breakdown voltage, BV_{CE0} , and a static current gain higher than 30. The available emitter lengths in that technology are 5, 7 and 10- μm , all were used in this circuit to get the best trade-off between footprint, thermal constraints and frequency response. This technology has three Au-based metallisation layers, thin film NiCr resistances and Si_3N_4 metal-insulator-metal capacitors. Additional information, including the fabrication process, can be found in [3].

Measurement set-up and results: A 2-port 110-GHz Anritsu ME7808A vector network analyser (VNA) was used to measure the standalone driver S parameters, from 70 kHz to 110 GHz, which are depicted in Fig. 2a. The single-ended gain, S_{21} , is 8.4 dB (14.4 dB differential) at 0.1 GHz and exhibits 6.2 dB of peaking gain at 59.4 GHz, which was useful to compensate for set-up bandwidth limitations during large-signal eye diagram measurements. A 106-GHz -3-dB bandwidth was obtained, together with a good input/output impedance matching, as S_{11} and S_{22} remain better to -10 dB up to, respectively, 92 and 100 GHz. But for the resonances that come from the passive parts modelling of the circuit and require adjustments, a good agreement between measurement and EM-circuit co-simulation is obtained.

Using the same VNA, the standalone linear driver single-ended output power versus single-ended input power characterisation was conducted at 1 and 30 GHz, as shown in Fig. 2b. The input/output 1-dB gain compression point is 1.8 dBm/9 dBm at 1 GHz, corresponding to a $3.56 V_{\text{pp}}$ differential output swing and testifying of a high linearity.

Those measurements also confirmed the equalisation capabilities of the linear driver as the power gain is increasing with the frequency.

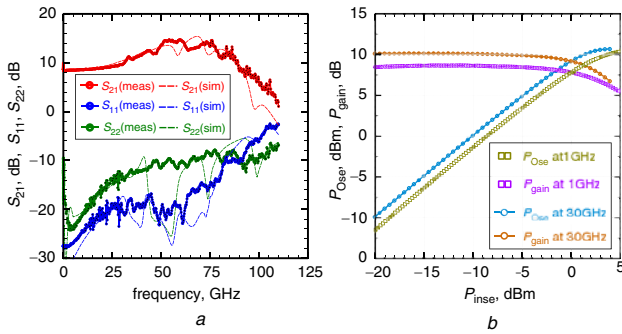


Fig. 2 Standalone InP linear driver characterisations

a S-parameter measurements (solid lines with symbols) and EM-circuit co-simulations (broken lines). The single-ended S-parameter gain, S_{21} , is displayed in red and the single-ended input/output S-parameter reflection coefficients, S_{11}/S_{22} , are, respectively, displayed in blue and green
b Single-ended output power (P_{Ose}) and power gain (P_{gain}) versus single-ended input power (P_{mse}). Measurements at 1 and 30 GHz are, respectively, displayed using square and circle symbols

Before large-signal eye-diagram measurements, to prevent signal degradations coming from cables and connectors, the linear driver has been placed on a mockup, as depicted in Fig. 1, and directly wire-bonded to an in-house InP active combiner, that generates high symbol-rate adjustable output amplitude PAM-4 signals from two NRZ inputs. Ribbons' width \times lengths are about $80 \times 300 \mu\text{m}^2$. Low ohmic RC-damped decoupling networks have been used on- and off-chip to bias both circuits. 40 Gb/s NRZ signals are generated using an Agilent E8257D synthesiser and a SHF 12100B bit pattern generator, those are then multiplexed, using an in-house InP 2 to 1 digital selector. A 65-GHz probe then feeds the 80 Gb/s NRZ signals to the active combiner, to generate 80-GBd PAM-4 signals. Two 70-GHz remote heads of an Agilent DCA-X 86100D sampling oscilloscope, used to observe the output signals, are connected to the linear driver's outputs through 65-GHz probes, DC blocks and 20-dB attenuators, to prevent any damage to the oscilloscope. Fig. 3 depicts very high-quality differential PAM-4 eye diagrams at the linear driver's output at 80 GbD. The active combiner's output signals are shown as insets in Figs. 3a and b, with an input amplitude of, respectively, 550 and 660 mV_{ppdiff}. Although no pre-emphasis nor digital signal processing was used, very high eye-diagram quality are obtained at the driver's output, thanks to its equalising capabilities that compensated for the bondings and the bandwidth limited output probing elements. Driver output eye diagrams with respective output swings of 2.55 and 3 V_{ppdiff} at 80 GbD testify of very high bandwidth and linearity.

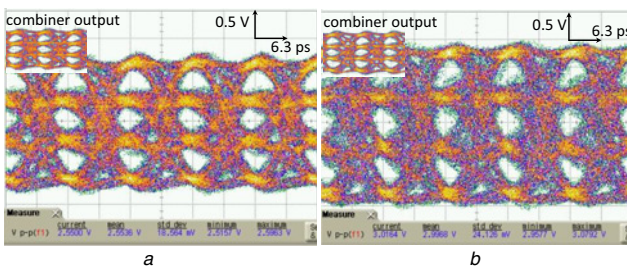


Fig. 3 InP linear driver differential 80-GBd PAM-4 output eye diagrams
a At a 2.55-V_{ppdiff} output swing with a 550-mV_{ppdiff} driver input (inset),
b At a 3.0-V_{ppdiff} output swing with a 660-mV_{ppdiff} driver input (inset)

State-of-the-art: Table 1 depicts transmitter circuit state of the art that conjugate over 1-V_{pp} output swing and over 64-GBd PAM-4 signals. To the best of the authors knowledge, the proposed linear driver has the highest gain-bandwidth product, as well as the highest figure-of-merit, as defined in (1), testifying of very efficient driving capabilities.

Table 1: High symbol-rate linear driver state-of-the-art

	[6]	[2]	[7]	This work
Material	InP	InP	InP	InP
technology	DHBT	DHBT	—	DHBT
−3 dB bandwidth, GHz	—	110	55	106
gain (S_{21}), dB	—	10.5	11	14.4
gain \times bandwidth, GHz	—	368	195	556
peaking gain, dB	—	8 ^a	—	6.2
peaking frequency, dB	—	85 ^a	—	59.4
PAM-4				
D_s , GBd	107	168	90	80
V_{opp} at D_s , V	3.7	1.5	3.2 ^a	3.0
Z_o , Ω	100	50	100	100
se ^b P_{O1dB} , dBm	—	—	—	9
f at P_{1dB} , GHz	—	—	—	1
P_{DC}/P_{DCOS} , W	2.9/1	0.99/−	3.6 ^d /−	0.74/0.45
FoM, GBd	0.6/1.8	0.95/−	0.32/−	1.22/2

^aEstimated values.

^bSingle-ended output power at 1-dB of gain compression.

^cPower consumption of the output stage.

^dModule P_{DC} .

Conclusion: This Letter presents the design and characterisation of a new linear lumped driver fabricated in the III-V Lab in-house InP 0.7- μm emitter width DHBT technology. Record gain-bandwidth product and figure-of-merit have been obtained together with a good linearity and low power consumption. It thus emphasises its high capabilities to very efficiently drive high-speed E/O modulators. Hence, this InP linear driver is paving the way to over 100-GHz E/O bandwidth transmitter for over 1 Tb/s/channel optical transceivers. Further exploration of this driver performances could lead to higher symbol-rate and PAM-8 characterisations, as well as long-distance very high symbol-rate optical transmission experiments.

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One or more of the Figures in this Letter are available in colour online.

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