Design, modelling and characterization of a 3-Vppd 90-GBaud over-110-GHz-bandwidth linear driver in 0.5-µm InP DHBTs for optical communications

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***Abstract*—In this article, we present the modelling, design and characterization of a 3-Vppd linear-output-swing 90-GBd PAM-4 modulator driver, realised in III-V Lab's in-house 0.5-µm InP DHBT technology (380/520-GHz f_T/f_{MAX}, 4.2-V BV_{CE0}). The driver exhibits 13-dB equalisation capabilities at 95 GHz with a bandwidth well beyond 110 GHz. It features a 0.67-W power consumption, resulting in a 1.5-GBd FoM with good output signal quality. To the best of our knowledge this linear driver shows the highest >64 GBd PAM-4 performance in current state-of-the-art, without DSP nor pre-emphasis. We also report on a newly developed 0.5-µm InP DHBT technology and its modelling using small-value external parasitic EM-simulation extraction, showing improved high-frequency prediction accuracy at circuit level.**

***Index Terms*—Large-swing linear modulator driver, high-speed integrated circuits, Tb/s optical communications, Indium Phosphide (InP) double heterojunction bipolar transistor (DHBT), 4-level pulse amplitude modulation (PAM-4)**

I. Introduction

Due to the exchanged data volume hyperbolic scaling, fostered by an unprecedented global video traffic, the need for an increased optical communication systems' capacity at reduced cost/bit as never been that high. Among the many potential paths to meet this challenge, conjugating increased electrical symbol rates with multi-level modulation formats, such as PAM-4, have proven interests, at the cost of stringent system requirements, and especially on signal-to-noise ratio (SNR). Targeting 100 GBd and beyond transceivers requires ultra-high performance integrated circuits, with analog bandwidth well in excess of 60 GHz.

Among those, the linear driver is key to maximise the optical-SNR while modulating the light carrier, through the electro-optical modulator, at such high symbol rates. Best-in-class Mach-Zehnder modulators have shown 1.5 to 2-V V_π with 80 to 100 GHz bandwidth to date. To conjugate high enough bandwidth and linear output-swing, while maintaining a low power dissipation, some research groups have traded footprint and integrability for distributed linear driver architectures. Respectively implemented in SiGe BiCMOS and Si CMOS, references [1] and [2] show 90- and 108-GHz bandwidth with 4-Vppd and 3.6-Vpp output swings while power dissipation is under 1 W. Yet published PAM-4 signals cap at 56 GBd and none provide equalisation. However, lumped architectures implemented in InP DHBT are capable of conjugating a higher integrability with >80 GHz bandwidths, high output swings, analog equalisation and limited consumption. In [3], an >110 GHz InP DHBT 1.5-Vppd 8-dB peaking gain analog multiplexer-driver with a 0.99-W power consumption enables a 168-GBd 16-QAM optical transmission, resulting in a 0.45-GBd driver FoM (as defined in equation (2)). Nevertheless, power-hungry DSP is required to reach this performance. Furthermore, based on III-V Lab's 0.7-µm InP DHBTs (see reference [4]), a 1.52-GBd-FoM, 86.8-GHz-bandwidth 4.1-dB peaking-gain linear driver with 4.9-Vppd PAM-4 output-swing at 50-GBd is presented in [5]. Besides, in [6], a 106-GHz-bandwidth 6.2-dB peaking-gain linear driver is shown, with a 3-Vppd PAM-4 linear output swing at 80-GBd, yielding a 1.22-GBd FoM without DSP.

In this article, a 3-Vppd linear-output-swing modulator driver running at 90 GBd in PAM-4 is presented, with a bandwidth well beyond 110-GHz and 13-dB equalising capabilities at 95-GHz. It relies on III-V Lab's in-house 0.5-µm InP DHBT technology. We also report on the 0.5-µm InP DHBT technology and its modelling approach using small-value external parasitics' electro-magnetic (EM)-simulation extraction, which compensates for the "over-de-embedding" typically associated with the standard S-parameter measurement de-embedding for triple-mesa InP DHBTs. This allows to alleviate many bandwidth-limiting layout parasitics and reach predictable high-speed circuit performances. Finally, this work shows a 1.5-GBd linear-driver-FoM, which, to the best of our knowledge, is the highest PAM-4 >64 GBd performance reported to date, while no DSP nor pre-emphasis was used. This result was enabled in conjugating a new driver architecture with downscaled DHBT and high accuracy modelling.

II. III-V Lab InP DHBT techonology

A. Device structure and process

The DHBT structure was grown on a 3-inch semi-insulated InP substrate by *IntelliEPI* using solid source molecular beam epitaxy. The intrinsic structure comprises a 40-nm InP emitter and a 28-nm compositionally graded InGaAs base. This layer is heavily C-doped (8×10^{19} cm^{-3}) leading to a base sheet resistance as low as 750 Ω/square, extracted from transmission

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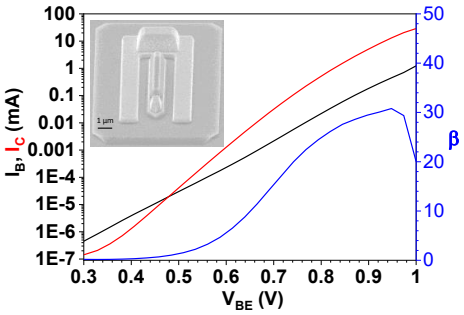

Fig. 1. Gummel plot at V_{BC}=0 V and static current gain (β) versus V_{BE}, of a 0.5×5-μm^2 InP DHBT. A transistor microphotograph, before interconnection level, is shown as inset.

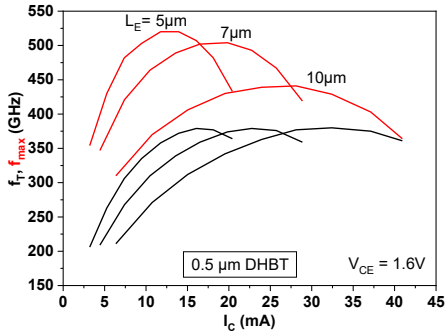

Fig. 2. 0.5-μm InP DHBT f_T and f_{MAX} for three emitter lengths

line measurements. A 130-nm thick collector is composed of a non-intentionally doped InGaAs spacer, a 25-nm thick heavily doped InP region and a lightly doped InP layer ($<2\times10^{16}$ cm^{-3}) to enable a high breakdown voltage. 0.5-μm emitter width InP DHBTs are designed with a rectangular shape and an emitter length varying from 5 to 10 μm. A 0.3-μm base contact extends on each side of the emitter and includes a plug for the connection. The transistors are processed using a wet-etched self-aligned triple mesa technology, as described in [4]. In comparison to previous hexagonal 0.7-μm DHBT, the 0.5-μm devices' footprint is halved, which minimises parasitic elements and enables much higher circuit-level density integration. A 0.5×5-μm^2 InP DHBT scanning electron microphotograph, before metal interconnection level, is shown as inset on figure 1. Transistors are included in a full circuit process, requiring up to twenty lithography steps. It comprises NiCr thin film resistors, SiN MIM capacitors and three Au-based interconnection levels, with polyimide as dielectric used in between.

B. Static and dynamic performances

As shown on figure 1, the 0.5-μm DHBTs features a maximum static current gain (β) exceeding 30. The common-emitter breakdown voltage BV_{CE0} is greater than 4.2 V at a 0.05-mA/μm^2 collector current density, J_C. As depicted on figure 2, maximum f_T and f_{MAX} of 380 and 520 GHz are respectively demonstrated at V_{CE}=1.6 V and $J_C\widetilde{=}$700 kA/cm^2 for a 5-μm emitter-length device.

III. InP DHBT Modelling

The large-signal model structure proposed for the InP DHBTs is shown on figure 3. It is based on the modified *UCSD*

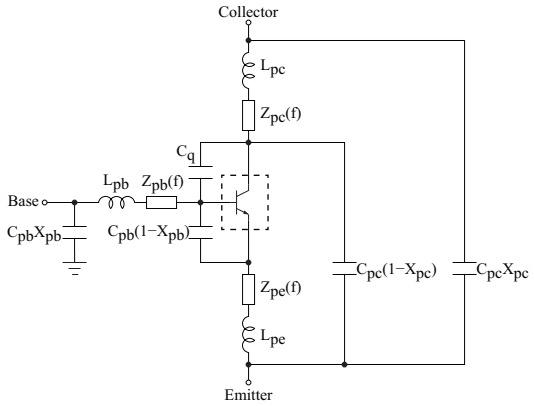

Fig. 3. Large-signal model structure for InP DHBTs. The dashed box contains the InP DHBT intrinsic part modelled using the modified *UCSD* HBT model

HBT model described in [7], embedded in an external parasitic network. The modelling of the parasitic effects related to the complete InP DHBT device structure becomes progressively more important as the circuit operation frequency are pushed well into the millimeter-wave frequency range. Unfortunately, it is nearly impossible to extract the small value external parasitic elements directly from measured S parameters. This is not only due to the uncertainty associated with measured S parameters at high frequencies, but also due to the fact that these external parasitic elements are often partly or completely removed by the de-embedding procedure, a process referred to as "over-de-embedding". The de-embedded S parameters used for small-signal model extraction thus do not contain the effect of these external parasitic elements. A more reliable procedure to extract the external parasitic network is to employ separate EM simulations on the complete device structure, see reference [8]. In this approach the reference planes for model extraction are kept at the access planes of the device structure by employing properly defined on-wafer calibration and de-embedding structures.

The *Ansys HFSS* 3D EM model employed for the extrinsic parasitic network extraction of the triple-mesa InP DHBTs is shown in figure 4. The access planes at the base, collector and emitters of the device are defined using lumped ports (orange sheets) referenced to the surrounding ground-ring. The excitation scheme with the surrounding ground-ring is preferred for InP DHBTs in a CPW test configuration. The parasitic effects associated with the lumped port excitations and surrounding ground-ring, however, have to be removed from the EM simulated results by an L-2L calibration procedure, see reference [9]. These effects would otherwise masks the small value external parasitic elements of the device structure itself. In the simulation, the active part of the InP DHBT is either short-circuited or left open-circuited. In the short-circuited device, the base, the emitter and the collector are all connected together using a shorting bar. The semiconductor layers within the active device structure are substituted by low dielectric constant ($\epsilon_r << 1$) layers in the open-circuited device. In this way the junction capacitances can be correctly allocated to the intrinsic device during the subsequent large-signal model parameter extraction procedure. Both structures are meshed at 325 GHz using an initial wavelength-based mesh setting of

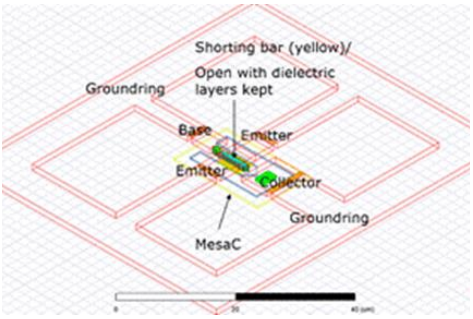

Fig. 4. *Ansys HFSS* 3D EM model of the complete triple-mesa InP DHBT structure with surrounding ground-ring. For clarity, the outer airbox and substrate layers are not shown.

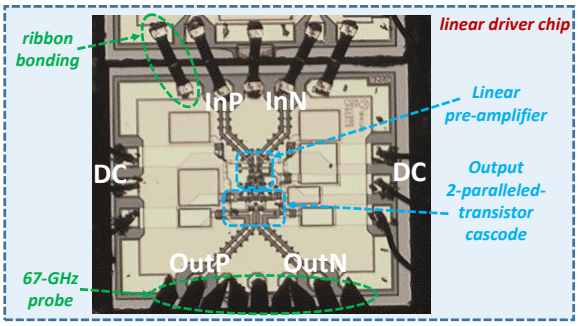

Fig. 5. InP DHBT linear driver chip micro-photograph mounted on an in-house mock-up together with a 2-bit in-house active combiner

0.03λ. To accurately capture the skin-effect due to the field penetration into conductors, an initial mesh seeding is employed and fields are solved inside. The simulated open- and short-circuited 3D EM structures allow frequency dependent effective capacitances and effective inductances, respectively, to be extracted. The distribution of these elements along the device structures follows a well-proven modelling procedure as described in [8]. For the triple-mesa InP DHBT device structures here considered, the external parasitic network takes on the rather complicated form as shown in figure 3. In this model, frequency dependent impedances are defined following equation (1).

$$Z_{pb(e,c)}(f) = R_{pb(e,c)}|_{f\to 0} + R_{pb(e,c),ac} \cdot \sqrt{f} \cdot (1+j) \quad (1)$$

Where f is the frequency, $R_{pb(e,c)}|_{f\to 0}$ are DC resistances and $R_{pb(e,c),ac} \cdot \sqrt{f} \cdot (1+j)$ are terms describing the ac impedance due to the field penetration into the conductors.

IV. Linear Driver Design and Performances

A. InP DHBT linear driver design

The linear driver has a two-amplifying-cell lumped architecture, composed of a pre-amplifier and an output stage. The pre-amplifier provides input impedance matching, voltage gain and common-mode rejection, achieved through two stages of emitter followers and a linear differential cascode amplifier that features emitter resistive degeneration and inductive peaking. The output stage is based on a 2-paralleled-transistor cascode differential architecture with resistive emitter degeneration, see [5], conjugating a very high gain-bandwidth product and a large linear output-dynamic. To further extend the bandwidth, ensure a good output impedance matching and provide high equalisation capabilities, inductive peaking is used in the output stage. Finally, to improve the overall bandwidth, an emitter-follower stage is interposed between the pre-amplifier and the output stage to mitigate the capacitive loading introduced by the paralleled-transistor topology.

The driver chip micro-photograph is shown on figure 5, its dimensions are 1.2×1.5 mm^2 while the core active region measures 0.32×0.4 mm^2. The driver total power dissipation is 0.67 W, of which 0.43 W originate from the output stage, hence corresponding to a 1.5-GBd driver FoM, and 2.4-GBd FoM for the standalone output stage, where the driver FoM is defined in equation (2).

$$\mathrm{FoM} = \frac{\mathrm{D_S} \cdot \mathrm{V_{Opp}^2}}{8 \cdot \mathrm{Z_0} \cdot \mathrm{P_{DC}}} \quad (2)$$

Where $\mathrm{D_S}$ is the PAM-4 symbol-rate, $\mathrm{V_{Opp}}$ is the single-ended or differential output swing at $\mathrm{D_S}$, $\mathrm{Z_0}$ is the single-ended or differential output impedance matching and $\mathrm{P_{DC}}$ is the circuit's DC power consumption.

A 3-Vppd linear-output-swing over-110-GHz-bandwidth lumped linear driver may not be obtained but for a fine modelling of the driver behaviour across the entire frequency range. This was achieved through intensive 2.5D EM-circuit co-simulation on *Momentum-ADS*. Based on the circuit's layout, a S-parameter model of all the passive elements is generated, and then used along with the DHBTs' large-signal model, to accurately account for the circuit's parasitics and behaviour, which helps in alleviating bandwidth limitations. This yields a very accurate model of the driver performances, as shown on figure 6 (section IV-B).

B. InP DHBT linear driver performances

The linear driver on-wafer (before wafer thinning and dicing) S-parameter measurements were conducted using a 2-port Anritsu ME7808A vector network analyser (VNA) from 70 kHz to 110 GHz. Figure 6 (a) depicts the driver single-ended S-parameter gain and input reflection coefficient. $\mathrm{S_{21}}$ shows a 6-dB (12-dB differential) low-frequency gain, together with -3-dB bandwidth (with respect to low-frequency gain) well beyond 110 GHz, exceeding the VNA upper bound frequency. A 13-dB inductive peaking gain is obtained at 95 GHz, hence showing higher equalisation capabilities and bandwidth than current state-of-the-art. Figure 6 (b) depicts the single-ended output reflection coefficient and the reverse gain S parameters. $\mathrm{S_{11}}$ and $\mathrm{S_{22}}$ respectively remain better to -10 dB up to 92 and 95 GHz, testifying of a broadband 50-Ohm impedance matching. $\mathrm{S_{12}}$ does not exceed -35 dB over 110 GHz, thus showing a good input/output isolation, which, together with the good impedance matching, improves the driver stability.

Besides, figure 6 presents a comparison of the driver measured and simulated performances, which simulation flow is described in section IV-A. One can note an accurate modelling of the linear driver behaviour, with enhanced precision above 50 GHz while using the proposed small-value external parasitic elements' extraction technique, compared to standard "over-de-embedding" sensitive procedures. This results

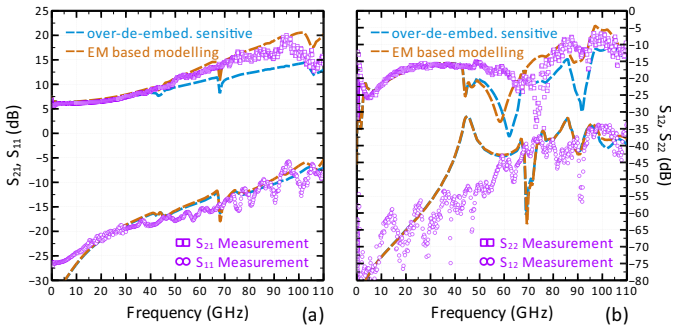

Fig. 6. InP DHBT linear driver single-ended S-parameter measurements. Measurements are displayed in magenta and EM-circuit co-simulation using the proposed modelling in orange and "over de-embedding" modelling in blue

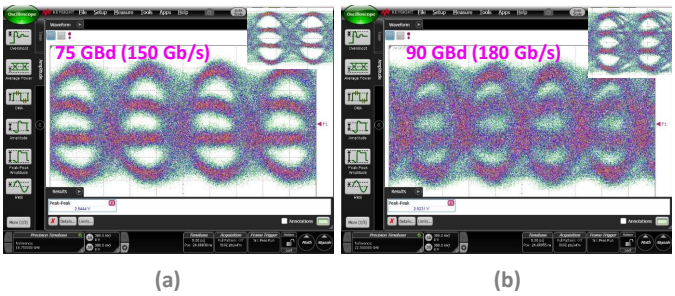

Fig. 7. InP DHBT linear driver differential PAM-4 output eye diagrams. (a) 3-Vppd 75-GBd (150-Gb/s) output signals, active combiner's 75 GBd output signal measured prior to connection with the driver shown as inset. (b) 3-Vppd 90-GBd (180-Gb/s) output signals, active combiner's 90 GBd output signal measured prior to connection with driver shown as inset

in a strong modelling improvement (mostly DHBT model) compared to previous works, see references [5] and [6]. A resonance occurs on simulated S_{12} and S_{22} around 41 GHz, yet strongly attenuated in measurement, which shows that some loss mechanisms may not be sufficiently accounted for in the EM simulation, which may be further improved. Moreover, the 73-GHz resonance experiences a 3-GHz frequency shift that may be related to an effective permittivity discrepancy. One should note that the InP wafer substrate is 600 µm thick, whereas the EM stack-up considers a 160-µm thinned substrate. The S_{22} low-frequency rise originates from a default in the VNA port 2 chain. Finally, the S_{11} low frequency measurement-simulation discrepancy indicates a small process variation during thin film NiCr resistance fabrication. For fair comparison, no post-processing, averaging nor retro-fitting was applied to measured and simulated data, only measured and simulated driver current consumption were matched.

To generate high-symbol-rate PAM-4 input signals with sufficient quality, after the InP wafer was thinned and diced, the driver chip was placed on a mock-up, along with an in-house InP DHBT 2-bit active combiner, as shown on figure 5. The chips were connected through 50-µm-wide, 300-to-350-µm-long gold ribbon bonding. All the mounting process was performed at III-V Lab. Driver's output signals were captured using a DCA-X 86100D sampling oscilloscope with two 122-GHz remote heads, connected to the chip through 67-GHz probes, 65-GHz DC blocks and 10-dB attenuators, protecting the sampling heads. Figure 7 (a) and (b) respectively depict the linear driver's output differential PAM-4 eye diagrams at 75 GBd (150 Gb/s) and 90 GBd (180 Gb/s) with a 3-Vppd linear output swing. A high quality eye diagram is obtained at 75 GBd, while some degradations can be observed at 90 GBd, of which a significant part may come from the ribbon bonding and the setup bandwidth limitations. One should note that active combiner's output signals were measured prior to connection to the driver chip and do not account for the ribbon bonding degradations. Additionally, no DSP nor pre-emphasis was used, thus, presented eye diagrams directly reflect the driver plus measurement environment raw performances.

V. Conclusion

This article reports on a 3-Vppd linear-output-swing >110-GHz-bandwidth 90-GBd (180-Gb/s) PAM-4 driver, implemented in III-V Lab's new 0.5-µm emitter width InP DHBT technology. To the best of the authors' knowledge, the linear driver shows the highest PAM-4 performances to date, without DSP nor pre-emphasis. Besides, the driver conjugates the highest bandwidth and equalising capabilities compared to other published > 2-Vpp linear drivers. We also report on the 380/520-GHz f_T/f_{MAX} 4.2-V BV_{CE0} 0.5-µm InP DHBT process and its modelling. Compared to traditional techniques that lead to "over-de-embedding", the proposed small-value external parasitic EM-simulation extraction procedure yields an improved high-frequency accuracy both at the transistors' and circuits' levels. This upgrade is critical for proper circuit operation at 90 GBd and beyond.

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