Towards wafer-scale integration of InP membrane photonics on InP substrates for high-speed datacenter applications

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In this paper, we discuss challenges faced towards wafer-scale co-integration of InP membrane photonics with InP electronics. We start by addressing thin film coatings for protecting the InP electronics wafer during wet etching removal of InP photonics wafer. We then investigate the evolution of BCB residual stress for different BCB thicknesses and treatment times. Finally, we assess the effect of residual stress of BCB and SiO_2 on the performance of HBT devices to validate the co-integration plan.

Introduction

Vertical co-integration of InP-based membrane photonics with InP-based electronics paves the way towards scalable compact high-speed devices. This technique relies on wafer-scale adhesive bonding and <20 µm long through-polymer vias gold interconnects to create a 3D monolithic circuit. Here, the sandwiched polymer ensures high thermal and electrical insulation while the gold interconnections drive the RF signal and acts as heat sink for photonics. This reduces the parasitic effects with increased device and interconnect integration density [1]

There are several challenges related to this integration scheme. First, we rely on wet etching and etch-stop layer to reach precise membrane thickness after bonding. For InP membranes on Silicon (InP), the chemical selectivity is high. Here, the InP electronics wafer itself is the carrier, thus high-quality hermetic protective coatings are needed to ensure the wafer is not damaged during the wet-etch of the InP photonics side. Secondly, BCB is cured during bonding at temperatures above 240°C. The resulting residual stress build-up need to be studied for different bonding conditions to ensure that the fabrication and performance of bonded devices on both sides are not affected.

In this paper, we discuss our investigation of these challenges starting by protective coatings for selective wet etching. We then discuss the residual stress of BCB *vs* BCB thickness and treatment time. Finally, we test the DC and RF performance of electronics undergoing this stress to validate the deasibility of this co-integration scheme.

Thin film protective coatings for InP wafer wet-etching

Wafer removal by wet etching is a key process to reach a InP membrane-thick layer for photonics with precise thickness. Etching is done using concentrated HCl at an extended time. For InP-InP bonded wafers, this requires backside protection to block the solution from damaging one of the substrates, e.g., the electronics wafer. The chemical reaction leads to forming concentrated PH_3 gas that can create or aggravate weak spots in the protective coating, which in-turn can complicate further processing. Thus, low-stress hermetic coatings are needed. Having these considerations in mind, we systematically investigated different combinations of protective layers. A schematic illustration of the tested coatings is shown in Fig.1. The pre-bond SiO_2 and ALD coatings are intended to

reach conformal coverage of the wafers sidewalls and increase hermicity, other coatings are used to strengthen the protection.

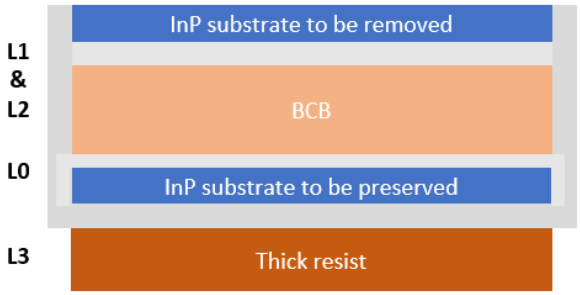

Figure 1: Schematic illustration of the layer stack. L:0-3 indicates the deposition order of these layers

We first investigated the required SiO_2 thickness for BCB adhesion before bonding (L0), the tested thicknesses are 50 and 500nm. Results show that 50nm thickness leads to BCB lift-off and higher damage to the InP wafer underneath. Therefore, 500nm thickness of the SiO_2 is required to fully encapsulate the InP wafer. Next, we investigated (<100Mpa) stress SiO_2 coatings on the backside (L1, L2). L1 is a thin 30 nm ALD-deposited layer that conformally covers the entire backside and wafer edges, while L2 is >1µm-thick SiO_2 to preserve the ALD-deposited SiO_2. Results show that both of these layers are required to fully preserve the wafer edges, while L2 is more flexible in terms of thickness. However, given that the wafers are extensively processed up to the point of bonding, SiO_2 protective coating were not sufficient to fully cover the backside due to the presence of particles. Therefore, an extra resist layer is needed to cover the surface.

Evaluation of residual stress in adhesive bonding

In this section, we assess the residual stress of BCB for unbonded wafers and relate it the post-bonding case. In adhesive bonding with soft-baked BCB, the BCB reaches a low viscous state and reflows before full curing. This reflow is ideal for planarizing structured interfaces. However, it also well accommodates for non-uniformities in the compression forces applied during bonding, which translates into large thickness non-uniformities [2]. For unbonded stacks, the BCB thickness non-uniformity after full cure is below 5%. Moreover, any mismatch in CTEs (coefficient of thermal expansions) between the two bonded wafers can contribute to this residual stress. Thus, we focused on the comprehensive study of residual stress of unbonded stacks to decouple these effects.

The evolution of BCB stress *vs* baking temperatures was previously studied [3]. However, the relationships between BCB stress and its thickness, and BCB stress and its treatment time have not been investigated. Hence, we fixed our treatment temperature at 280 °C and studied these relationships to have a full view on bonding-induced residual stresses. The investigated thickness range is 1-16 µm, whereas the treatment time range corresponds to 95% crosslinking to well beyond full crosslinking. We also used Si and InP carriers for higher accuracy. The stress is assessed by measuring the variation in wafer bow. We used Stoney's formula to extract the stress values given by [4]:

$$\sigma = \frac{E_s}{6(1-v_s)}\frac{h_s^2}{h_f^2)}\left(\frac{1}{R}-\frac{1}{R_s}\right)$$

Here, E_s and v_s are the Young modulus and Poisson ratio of the substrate, h_s and h_f are the thicknesses of the substrate and deposited thin film, and R_s and R are the substrate curvature radius before and after deposition (or thermal treatment in some cases of this study). The bow profiles are measured using profilometry and automatically fitted to

extract accurate bow values. The process flow consists of cleaning the wafers and depositing and outgassing 50 nm SiO_2. BCB is then deposited and cured for different periods. The bows are tracked between each deposition or curing step. The BCB thickness is tracked with reflectometry. We measured bows in both directions perpendicular and parallel to the wafer major flat to increase the accuracy. The average bow of the two directions are plotted for each thickness and curing time for Si and InP carriers in Fig.2.a) and Fig.2.b), respectively. We identify each wafer by its BCB thickness after the full cure. The dashed line represents the stress expected from CTE mismatch between BCB and the carrier wafer given by:

$$\sigma = \left(\frac{E_{BCB}}{1 - \nu_{BCB}}\right)(\alpha_{BCB} - \alpha_{carrier})\Delta T$$

Where E_{BCB} and ν_{BCB} are the Young's modulus and Poisson ratio of BCB, α_{BCB} and $\alpha_{carrier}$ are the coefficients of thermal expansion of BCB and the carrier wafer, and ΔT is the temperature window.

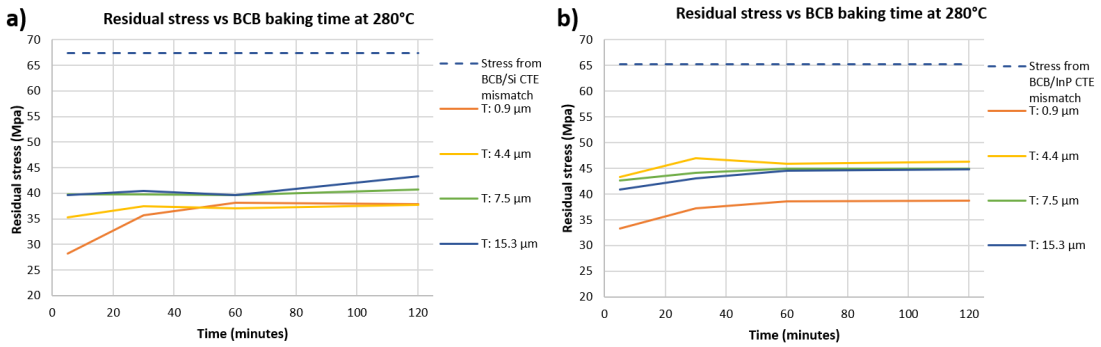

Figure 2: Residual stress *vs* baking time for different BCB thicknesses for: a) Si carrier, b) InP carriers

Results show the residual stress is tensile-strained, because of the higher stretching and contracting of BCB. From Fig.2, it can be seen that the residual stress values are similar for various BCB thicknesses. All of these values are below the stress expected from CTE mismatch between BCB and the carrier wafer, signifying a partial stress relaxation given the mobility of polymer chains at this temperature, which is also in agreement with results from [3]. The stress increases with increasing treatment time in the range of 5 to 30 minutes and then stabilizes, signifying that the polymer chains are no longer mobile and the full cure is achieved between 5 and 30 minutes when BCB is treated at 280°C. These findings also suggest that the residual stress is mainly dominated by the CTE mismatch between BCB and the carrier wafer, which is in-turn is dominated by the large thermal expansion of BCB compared to any other solid-state substrates. Here, the difference in obtained stress values for Si and InP carries is below 10 MPa. Therefore, in the case of InP-Si or InP-InP bonding, we expect the stress values to be similar to or lower than these values regardless of the high BCB non-uniformities after bonding.

Effect of SiO_2 and BCB residual stress on InP electronics performance

To validate the possibility of this co-integration scheme, we tested the performance of HBTs under this residual stress. For this, we received two InP HBT samples from III-V Lab. We tested the stress of 500 nm SiO_2 as reference (required as protective coating), and compared it to adding 12µm BCB after full cure (required for planarization). We used the same flow as discussed before and photolithography to open only the pad areas as shown in Fig.3. Devices are then characterized for their DC and RF performance.

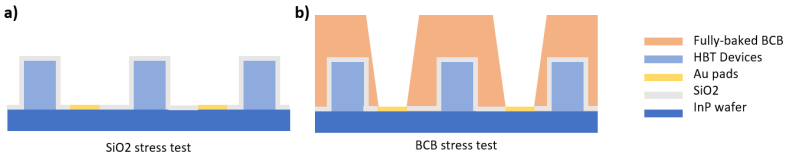

Figure 3: Schematic representation of the stacks dedicated for testing the stress of: a) SiO_2, b) BCB

Based on our previous investigations, temperatures for thermal treatments on HBTs need to be lower than 250°C to avoid significant performance degradations. Therefore SiO_2 outgassing and BCB full-cure both required baking at 240°C for 10h.
DC and RF characteristics of several tested HBTs are shown in Fig.4.

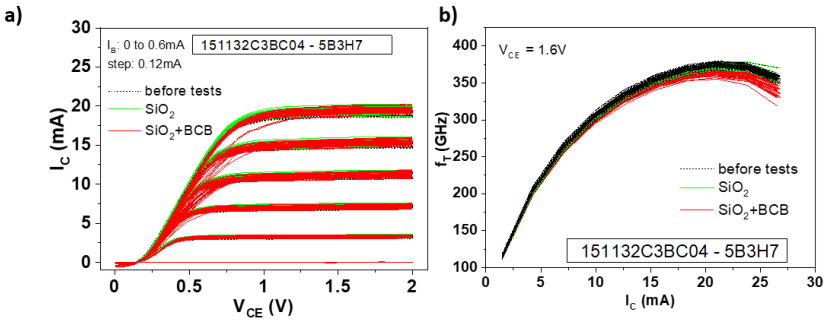

Figure 4: a) DC and b) RF characteristics of HBTs before and after adding SiO_2 and SiO_2 +BCB. Number of characterized transistors: 80 before tests, 26 after SiO_2, 36 after SiO_2 +BCB

Measurements on the SiO_2 sample showed that the transistors were not affected by the deposition while ones performed on SiO_2+BCB showed a slight degradation of the transistor emitter resistance, and thus f_T. This degradation is linked to the hard baking conditions used for BCB with double the thermal budget delivered to the first sample.

Conclusions

To conclude, we investigated processing steps for co-integration of InP electronics and photonics. Using 500nm SiO_2 before bonding and multi-coatings on the backside is optimal as protective coating. The residual stress of BCB is mainly dominated by BCB/substrate mismatch, regardless of the treatment time and BCB thickness. BCB partial stress relaxation yields values below 50 MPa. This stress had no effect on the performance of HBTs, thereby further validating our co-integration plan.

Acknowledgements

This work was supported by the H2020 ICT TWILIGHT Project (contract No. 781471) under the Photonics PPP.

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