

# Design optimization and fabrication tolerance analysis of a polarization insensitive spot-size converter for InP-membrane-on-silicon platform

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## Abstract

*We report on the design optimization and fabrication tolerance analysis of a broadband, low-loss and polarization insensitive integrated fiber-to-chip coupling spot-size converter(SSC) on InP-membrane-on-silicon (IMOS) platform. The proposed SSC consists of a laterally tapered InP waveguide and a SiN secondary waveguide. The fundamental TE-polarized and TM-polarized mode is efficiently converted from the high-confinement single-mode InP waveguide with the cross-section of  $0.4 \mu\text{m} \times 0.3 \mu\text{m}$  to the low-confinement SiN waveguide with a cross-section of  $4 \mu\text{m} \times 3 \mu\text{m}$  via a lateral InP taper. The calculated transmittance for TE-fundamental mode is up to 97.2% and 84.5% for TM-fundamental mode (from InP to SiN). The influence of the fabrication error, e.g., the critical dimension deviation of the InP taper, the spatial misalignment of the SiN secondary waveguide with respect to the InP taper, and the verticality of SiN waveguide side-wall, has been numerically analyzed via eigenmode expansion (EME) method.*

## Introduction

Polarization insensitive, broadband, efficient chip-to-fiber coupling remains to be challenging to integrated photonics. Silicon photonics offers low-loss, compact edge couplers[1-3] but lacks high-performance, native amplifiers and modulators, which hinders the integrity of the photonic integrated circuit (PIC). The conventional III-V technologies can provide monolithic integrated photonic system but lacks broadband, polarization independent chip-to-fiber couplers, which however is important in modern high speed telecom industry. A novel InP membrane platform, on which the light can be confined into the compact waveguide, can offer monolithic integration solution with its native active photonic components[4-5].

In this work, we report on the design optimization and fabrication tolerance analysis of an integrated index-matching SSC on InP-membrane-on-silicon (IMOS).

## Design Optimization

The proposed SSC consists of an adiabatic inverse InP taper as the core, and a bulk SiN secondary waveguide as the low-index cladding waveguide, as shown in Figure 1(a-b). The wider side of the inverse InP taper connects to the IMOS waveguide, while the narrower side (tip) points towards the chip facet. A SiN bulk waveguide covers the InP taper and ends at the chip facet. As shown in Figure 1(c), the mode propagates from IMOS waveguide will be compressed when the light is going through the inverse InP taper, as the taper cross-section is gradually shrinking. When the InP taper becomes too small to sustain the mode, the mode will partially distribute in the outer region of the InP taper and confined in the SiN waveguide, which has a larger cross-section but smaller index contrast to the surrounding (usually air or polymer). Till then, the modal size conversion from a high-confinement nano-waveguide ( $0.4 \times 0.3 \mu\text{m}^2$ ) to a low-confinement bulk waveguide ( $4 \times 3 \mu\text{m}^2$ ) is completed.

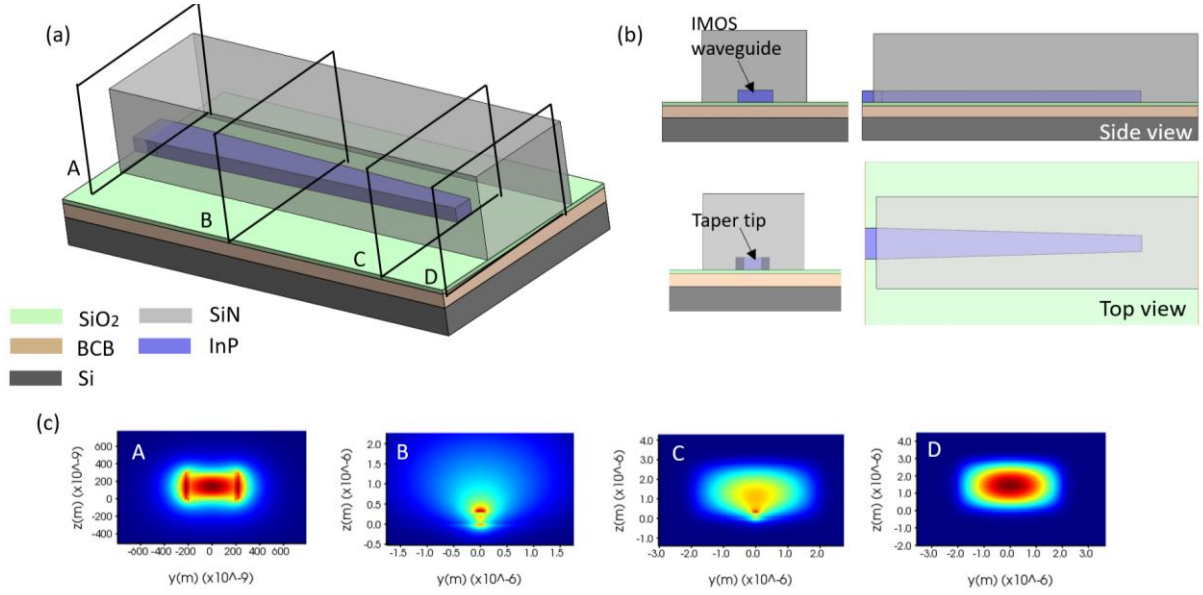


Figure 1: (a) the 3D demonstration (not-to- scale), (b) the orthographic projection (not-to-scale) and (c) the mode slices of the proposed SSC (note that scales are different in the four slices)

There are several design parameters which can essentially influence the mode conversion efficiency of an SSC from design aspect, namely the width of the taper tip, the lateral slope of the taper and the dimension of the SiN waveguide cross-section. Each of these parameters has been systematically studied for fundamental TE and TM mode via eigenmode expansion (EME) method and will be introduced in the following. To define the terminology, the conversion efficiency in this paper refers to the transmittance when the InP waveguide mode adiabatically converts to the SiN waveguide mode. Polarization conversion will not be discussed if not specified.

A joint study on the tip width and the taper length has been performed in this work, the tip width varies from 200 nm to 50 nm with a step-size of 50 nm, and the length of the taper is swept from 1  $\mu\text{m}$  to 401  $\mu\text{m}$  with a step-size of 10  $\mu\text{m}$ . Figure 2 reveals the tip width dependency and the lateral slope dependency of the conversion efficiency for both fundamental TE and TM mode. Both plots clearly prove that longer taper is preferable in a SSC because of lower optical loss in propagation. For fundamental TE mode, the maximum conversion efficiency is only 40% when the tip is 200 nm wide, but it can be significantly improved to 97% by narrowing the tip down to 150 nm. For TM fundamental mode, the conversion efficiency reaches 85% when the tip width is below 100 nm. In order to achieve balanced efficiency for both fundamental TE and TM mode, and also to take the fabrication feasibility into consideration, the optimal tip width is set to be 100 nm in this design.

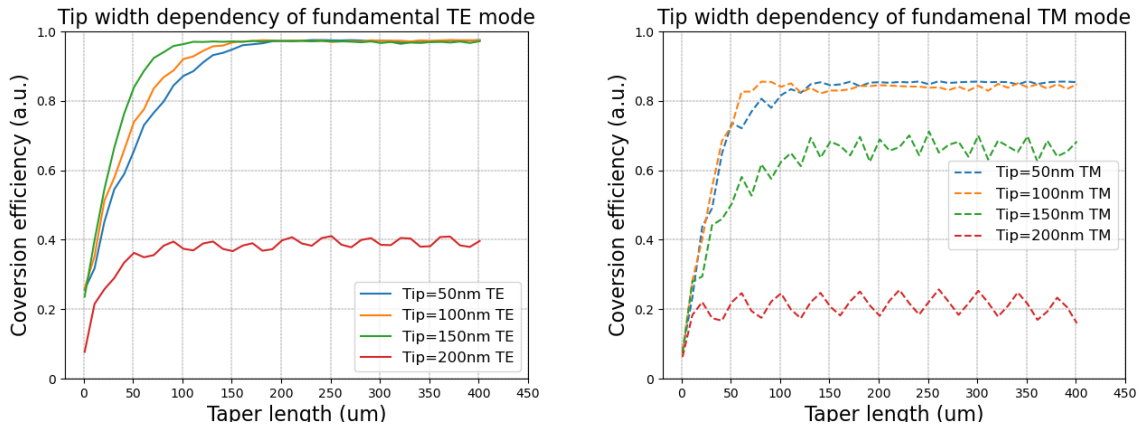


Figure 2: the tip width dependency of the conversion efficiency of the fundamental TE mode (left) and of the fundamental TM mode (right)

The dimension of the SiN waveguide determines the mode distribution inside the SiN waveguide. Considering the modal size in the off-chip coupling devices (fibers, couplers, etc.) is usually larger than  $3\ \mu\text{m}$ , and the output facet of SSC should match to the off-chip couplers. Hence, designs with varying cross-section with minimal dimension of  $3\ \mu\text{m}$  have been verified in EME simulation. The design of InP taper has been fixed as  $100\ \text{nm}$  according to the results introduced above. The InP taper length is set to be  $200\ \mu\text{m}$ , to compromise the foot print of SSC and its conversion efficiency. The simulation results plotted in Figure 3 reveal that  $4\ \mu\text{m} \times 3\ \mu\text{m}$  (*width*  $\times$  *thickness*) is an optimal design choice which balances the conversion efficiency of the fundamental TE and TM mode. The wavelength dependence is plotted in Figure 3, bottom, showing a broadband up to  $300\ \text{nm}$ .

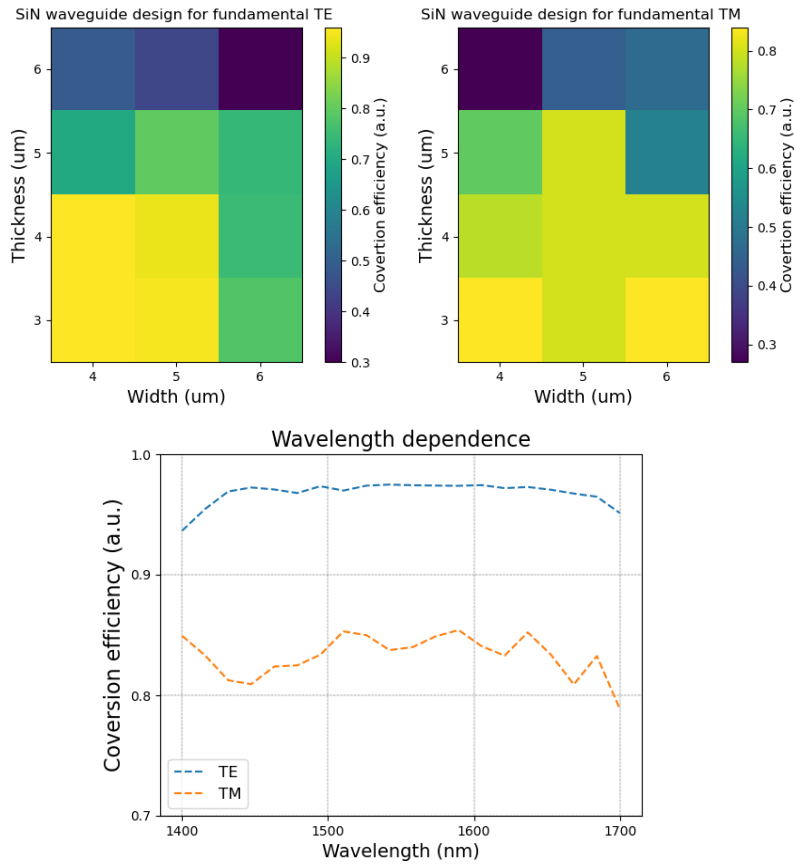


Figure 3: SiN waveguide cross-section dimension analysis for fundamental TE (top left) mode and fundamental TM mode (top right) and the wavelength dependence of the optimum design (bottom)

## Fabrication tolerance analysis

The fabrication tolerance analysis in this work is mainly focused on three aspects: the critical dimension (CD) tolerance of the InP taper tip width, the sidewall verticality of the SiN waveguide, and the spatial misalignment between the InP taper and the SiN waveguide.

The deviation in CD is inevitable during fabrication, as the fabricated structure can suffer from CD loss in any uncalibrated process step. And the CD loss is usually in the order of a few nanometers. Therefore, we set up a small range modification ( $\pm 5\ \text{nm}$  and  $\pm 10\ \text{nm}$ ) around the optimum design width ( $100\ \text{nm}$  in this work), to emulate the CD loss during fabrication.

As shown in Figure 4, the change of the conversion efficiency, which comes from tip width small variation, is ignorable for both fundamental TE and TM modes.

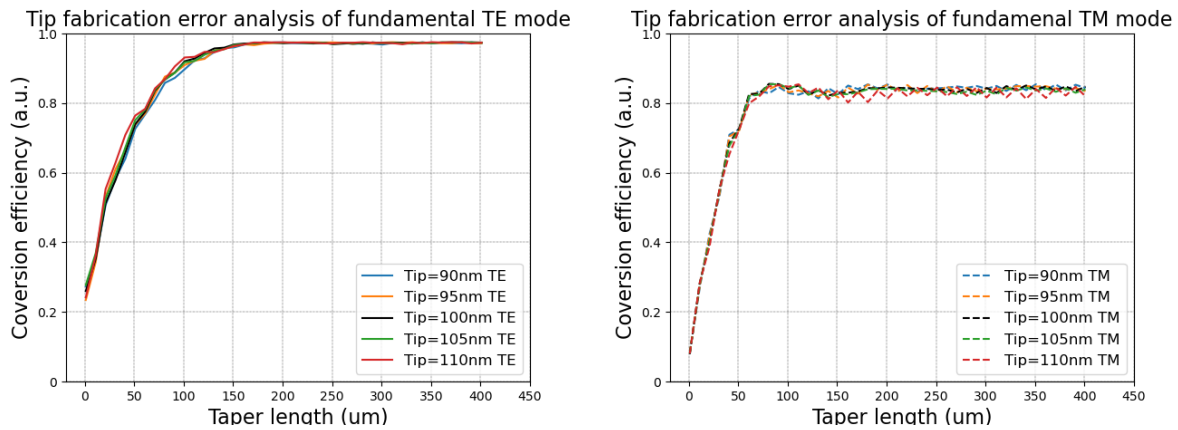


Figure 4: tip width CD tolerance analysis for fundamental TE (left) and TM (right) mode

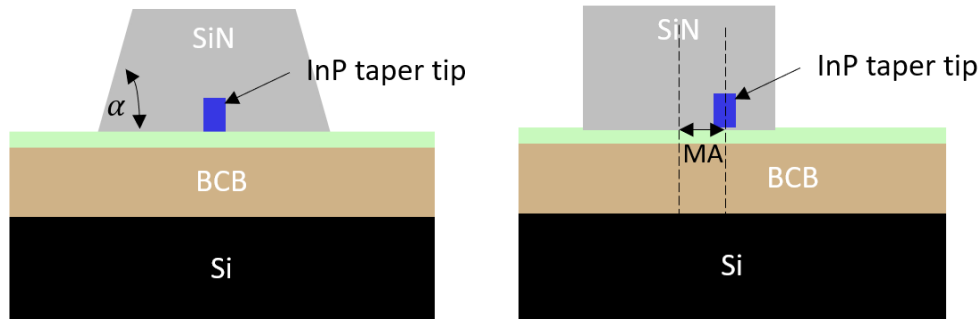


Figure 5: the schematic demonstration of the sidewall non-verticality (left) and the spatial misalignment of the SiN waveguide with respect to the InP taper

The influence of a sloped SiN sidewall has been investigated by varying the geometric model of the SSC in EME simulation. The sidewall angle  $\alpha$  varies from  $45^\circ$  to  $90^\circ$  (vertical) with a step-size of  $15^\circ$ , as shown in Figure 5, left. The width of the taper tip is fixed as  $100\text{ nm}$ . The results are plotted in Figure 6. As we can see in the left plot in Figure 6, the conversion efficiency of the fundamental TE mode fluctuates a lot when the sidewall angle is  $45^\circ$ , which is an extreme case for an unsatisfied sidewall verticality. When the sidewall angle is beyond  $60^\circ$ , the TE mod conversion becomes stable. Compare with the best-case scenario, i.e., the waveguide with perfectly vertical sidewall ( $\alpha = 90^\circ$ ), a  $15^\circ$  deviation on sidewall is tolerable for the fundamental TE mode, as its conversion efficiency doesn't differ much. For the fundamental TM mode, the proposed SSC can tolerate even more verticality deviation, as the electric field of a TM mode oscillates vertically in the waveguide, thus a TM mode is less sensitive to the lateral sidewall. As shown in the right plot in Figure 6, the modal conversion efficiency of SSCs with different sidewall angle shows very high consistency when the taper length is above  $150\ \mu\text{m}$  and no evident efficiency degradation is observed.

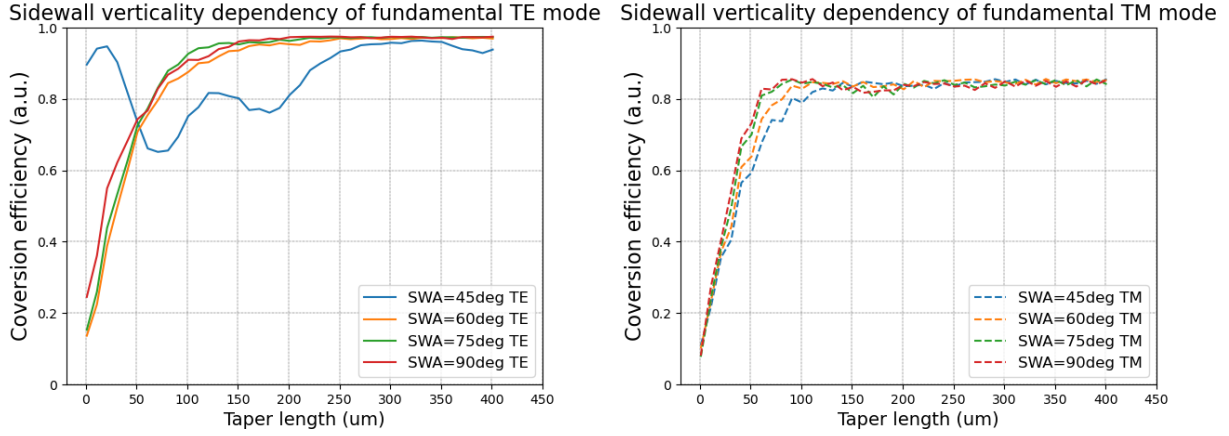


Figure 6: the sidewall verticality dependency of the conversion efficiency of the fundamental TE mode (left) and of the fundamental TM mode (right)

To investigate the spatial misalignment tolerance of the proposed SSC, an offset between the SiN waveguide and the InP taper is introduced, as shown in Figure 5, right. The offset varies from 0 to  $1.8 \mu\text{m}$  with a step-size of  $0.45 \mu\text{m}$ . The width of the taper tip is fixed as  $100 \text{ nm}$ . As indicated in both plots in Figure 7, the conversion efficiency for both fundamental modes degrades enormously when the SiN waveguide is  $1.8 \mu\text{m}$  off from the InP taper, in which case the InP taper locates at the edge of the SiN waveguide. Despite this extreme case, the proposed SSC shows acceptable spatial misalignment tolerance, namely  $0.45 \mu\text{m}$  for fundamental TE mode and  $0.9 \mu\text{m}$  for TM mode.

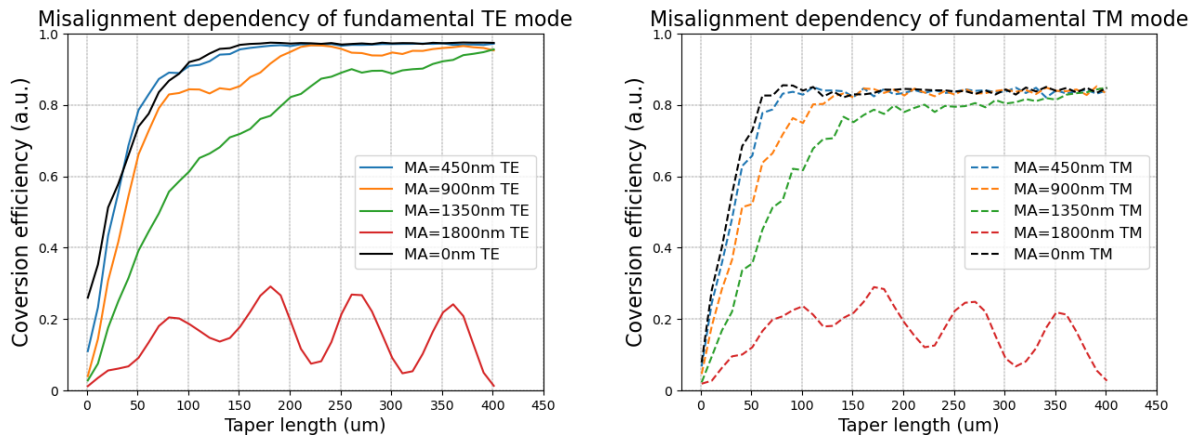


Figure 7: the spatial misalignment tolerance of the SSC in the case of fundamental TE mode (left) and of the fundamental TM mode (right)

## Conclusion and outlook

In this work, we designed and optimized a polarization insensitive broadband SSC for IMOS platform. The fabrication tolerance analysis proved its feasibility. This design will be further verified in an on-going IMOS MPW fabrication run. In the future, further study will be performed to increase the conversion efficiency of the fundamental TM mode.

## Acknowledgement

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