140 Gb/s WDM Data Routing in a Lossless Strictly Non-Blocking SOA-Based Photonic Integrated 8×8 Space Switch

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Abstract: We demonstrate 4×35 Gbps error-free WDM data routing in a lossless compact 8×8 InP optical space switch with 2 dB worst-case penalty. 10 dB IPDR within 1.5 dB power penalty is measured at 12.5 Gbps.

1. Introduction

Driven by mobile application growth, cloud-based virtual services and high definition video service, the global IP traffic is growing fast and a large volume of it touches data centers [1]. More importantly, the traffic exchange in a datacenter is immensely significant than inbound/outbound traffic [2]. Its behavior has also been changing dictated by the burst nature of the traffic, demanding fast and dynamic network readaptation. This requires network switches with high speed and capacity. Electronic switches have started struggling with this demand: Scaling is challenging because of switch ASIC power consumption and bandwidth limitation [3]. A paradigm shift in data center architecture from electronic switch based hierarchical network to optical switch based flat network has been proposed to take advantage of photonic features [4]. Semiconductor optical amplifier (SOA) based switches are potential candidates for flat network architectures, as they leverage the high bandwidth and nanosecond scale switching capability of SOAs. However, amplified spontaneous emission (ASE) building up from cascading SOAs [5] and limited input dynamic range (IPDR) limit their scalability in wavelength division multiplexed (WDM) operation.

We have recently demonstrated an 8×8 optical space switch with lossless operation, extinction ratio (ER) and optical signal to noise ratio (OSNR) higher than 35.0 and 40.0 dB, respectively, and an output saturation power of 8 dBm in continuous-wave operation [6]. These figures hint at the possible usage of these switches for multi-channel data routing with good signal integrity. In this paper, we present WDM data signal routing through this 8×8 WDM space switch. We investigate the high-power operation, crucial for WDM applications, by measuring the IPDR, and we evaluate signal integrity by measuring the bit error rate (BER) for 4×35 Gb/s multi-channel data.

2. Photonic integrated circuit design and architecture description

The designed circuit includes co-integrated SOAs and passive components via an active-passive integration scheme on the InP material-based wafer and occupies the space of two generic InP cells (each cell is 4.6×4 mm^2) fabricated by the SMART Photonics foundry [7]. Fig.1 (a) shows the fabricated and wire-bonded chip, while fig. 1(b) shows its layout designed with broadcast and select architecture shown in fig. 1(c). The broadcast functionality is implemented by a 1:8 splitter per port designed with 7 1:2 multimode interference (MMI) splitters cascaded in a tree topology. Every waveguide from the splitter at each input port is connected to every waveguide of the combiner at each output port via a gate SOA, creating 64 independent paths. Each input port has one SOA before the correspondent splitter to serve as a booster, while each output port has one SOA after the correspondent combiner to serve as a preamplifier: This is done to compensate for the path losses. This architecture requires $N^2 + 2N$ SOA and $2N(N-1)$MMIs for an N×N switch, where N is switch radix, meaning that we have 80 SOAs and 112 MMIs integrated within the switch circuit. The presence of 6 MMIs in each optical path contributes up to 21 dB loss. With at least 10 dB gain per SOA and three SOAs per path in this architecture, it is possible to compensate splitting/combining and other path loss, making this a very suitable architecture choice for an 8×8 I/O connectivity. However, as port count increases, we may need to use longer SOAs or different multistage architectures to meet lossless operation.

In the design phase, we have introduced two novel design approaches. On the one hand, whispering gallery mode micro-bends specifically designed for the InP platform are utilized to realize steep waveguide bends (20 μm radius) to increase the circuit compactness [8]. Moreover, since the active gain region carriers become depleted as the input optical power increases, resulting in non-linearity effects (such as a decreased gain and power saturation) detrimental for WDM operation, we design the on-chip SOA waveguides with a wider width of 3 μm: The output saturation power, $P_{(o,sat)}$ and the SOA amplifier modal area are, in fact, directly proportional [9, 10], suggesting that a slightly wider

SOA active waveguide can increase the output saturation power for enabling WDM operation. For our 450 μm long SOA, we manage to achieve 8 dBm output saturation power.

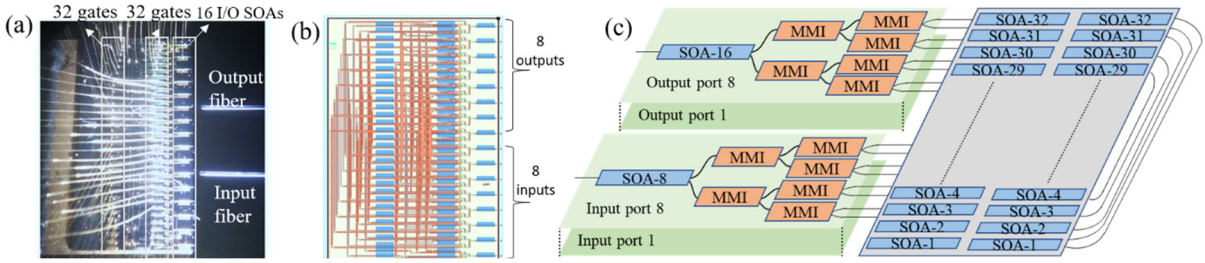

Figure 1 (a) Fabricated and wire-bonded chip. (b) Mask layout of the switch. (b) Detail architecture of the switch.

3. Experiments and results

A testbed has been set up, as shown in Fig. 2 (a), to assess the switch experimentally. The optical chip is mounted on a water-cooled heat sink and operated at 18 °C. Four optical channels at wavelengths λ_1=1549.32 nm, λ_2=1550.92 nm, λ_3=1552.52 nm, and λ_4=1554.13 nm, on ITU grid with channel spacing of 200 GHz, are generated from a laser array. The CW optical signals are individually connected to a polarization controller and then combined by a 4:1 combiner, before being fed to an SHF transmitter for modulation. The light is modulated with non-return to zero on-off keying (NRZ-OOK) data of pattern length 2^{31}-1, amplified, decorrelated, polarization controlled and input to the chip via a lensed fiber mounted on a 3-axis stage. A multi-channel current controller is used to bias the booster, gate and preamplifier SOAs of each path with a suitable current level (in the range 40-70 mA) to route the signal to the desired output port without loss, but still with a reasonable OSNR. The output signal is coupled back into a lensed fiber, amplified, demultiplexed and fed to the BER tester. The current controller, the optical spectrum analyzer and the attenuator are connected to a computer through a GPIB cable for automatic setting and data acquisition.

The spectrum of the WDM data signal at the switch input is compared with the WDM data signal spectrum at the chip output, as shown in fig. 2(b). We observe around 20 dB noise floor increase at the output because of the ASE build-up from the three cascaded SOA, which added to the coupling losses, causes the OSNR to decrease from 60 dB down to 30 dB. Nevertheless, we see that our chip fully overcomes the on-chip losses, as initially predicted. Specifically, the 9 dB coupling loss arising from both chip facets forces us to amplify the output signal to the SHF receiver with -14 dBm sensitivity, adding additional noise that hence depends on the setup power budget limitation. Fig. 2(c) shows the spectrum of the signal fed to the receiver after amplification and demultiplexing via external AWG.

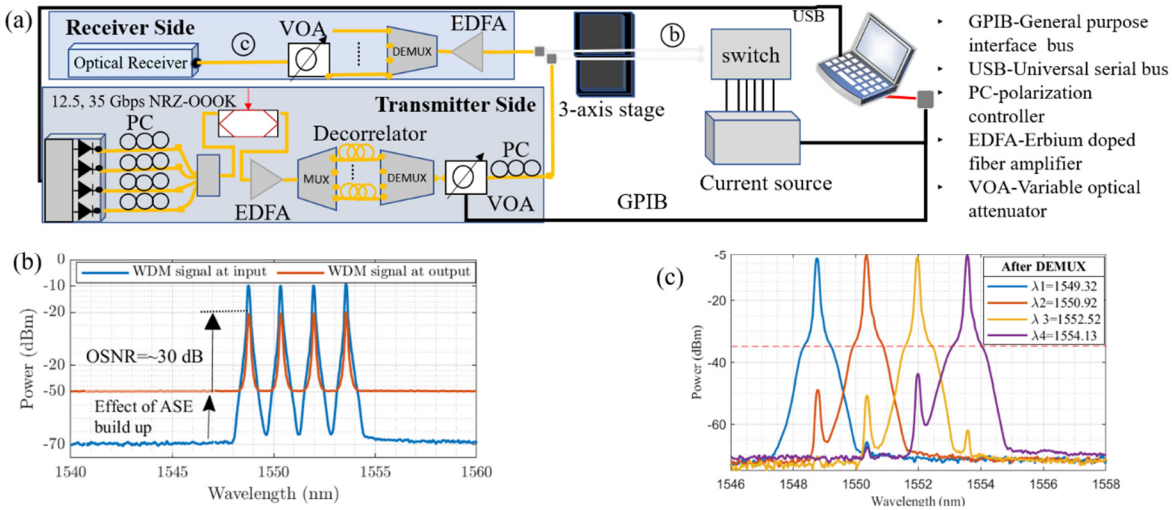

Figure 2: (a) Experiment setup. (b) Transmitted and received WDM optical signal. (c) Spectrum of the demultiplexed signal at receiver.

Fig. 3 (a) shows the power penalty measurement for different input powers at 12.5 Gbps, since the current setup power budget does not allow IPDR measurements at 35 Gb/s. We measured a best-case error-free transmission with a power penalty of less than 0.3 and an IPDR of around 10 dB at 1.5 dB power penalty. From the IPDR plot, we can see that the power penalty rises on the low- and high-power side due to OSNR degradation (when power is decreasing) and to the increasing non-linearity (when the power is increasing), respectively. Only the booster SOA may operate

in the nonlinear region as the other SOAs receive low input power due to path loss. The red dotted curve in the graph portrays the gain for the booster SOA: As power increases, the gain decreases, explaining an increase in power penalty.

Fig. 3 (b) shows the BER curves for the routed NRZ-OOK WDM 4 channel-signal at 35 Gbps line-rate/channel measured for the representative path from input 6 towards output 3. All received channels offer error-free routing at a 10^{-9} BER with a worse case 2 dB power penalty for λ_4. The performance from channel to channel at the same bit rate does not show a significant difference: The SOA performance does not significantly vary over 6.4 nm bandwidth. We expect it is possible to add more channels when the setup power budget allows us to fully exploit the broadband nature of the SOAs. From fig. 3(c), we observe that the BER is higher at a higher bit rate due to the increased non-linearity effect. Overall, the results received for BER and IPDR are the best reported so far for an SOA-based 8×8 switch fully integrated on-chip. Better performance has been anticipated by connecting 2×2 hybrid MZI-SOA switches to achieve an 8×8 connectivity [11], however, our chip additionally allows 3 times improved compactness, broadband operation and ease of electrical control (with 3 times less electrodes).

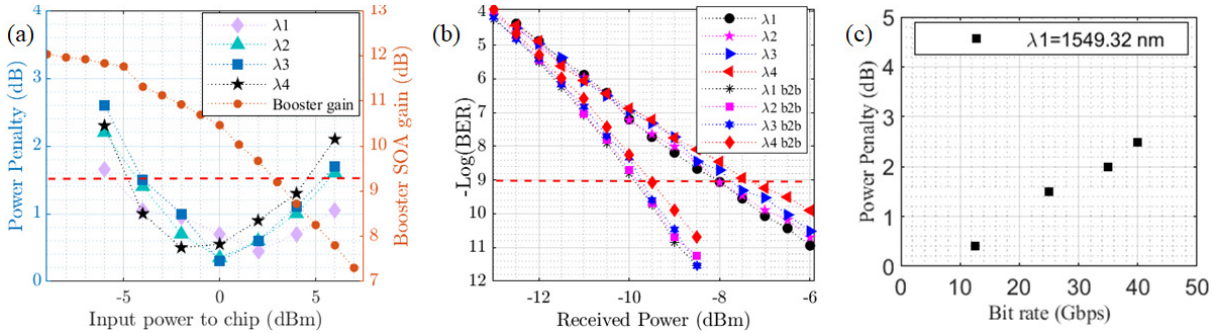

Figure 3 (a) Input power dynamic range at 12.5 Gbps. (b) Bit error rate versus received power for each channel at 35 Gbps. (c) Power penalty versus bit rate (all measurements are for NRZ-OOK at BER=10^{-9}).

4. Conclusions

In this work we present a 3 SOA stage 8×8 photonic integrated optical space switch and experimentally demonstrate error-free data signal routing with four NRZ-OOK modulated and multiplexed channels up to a bit rate of 35 Gbps per channel at BER=10^{-9}, with similar performance for all channels. An IPDR of 10 dB at 12.5 Gbps is measured within 1.5 dB penalty, showing that this architecture, combined with the exploited more resilient SOA design and ultra-compact micro-bends, can achieve good signal integrity for WDM operation over a wide input power range in a very compact footprint. The setup power budget mainly limits the switch scalability investigation: A higher sensitivity receiver would allow more channels through and at higher line-rates. For higher switch connectivity, multistage architectures such as Banyan and Benes may be used on a modular basis to get improved OSNR and power penalty metrics.

Acknowledgments

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