112 GBaud (224 Gb/s) large output swing InP DHBT PAM-4 DAC-driver

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***Abstract* — In this paper, we report on the design, optimisation and and electrical measurements of a PAM-4 DAC-driver fabricated in 0.7-µm InP/GaAsSb DHBT technology, with the capability to directly drive an electro-optical modulator. Circuit measurements in PAM-4 mode show high diagram quality at 90 GBaud (180 Gb/s) with a record 5.5–V_{pp} differential output swing. An over 12-dB gain control capability is shown. Moreover, a record 3.35-V_{pp} output swing is obtained in PAM-4 at 112 GBaud (224 Gb/s). Power consumption is 1.1 and 0.6 W for two operating symbol-rates respectively.**

***Keywords*—modulator-driver, integrated circuit (IC), Indium Phosphide (InP), Double Heterojunction Bipolar Transistor (DHBT), high speed circuits, optical communications, PAM-4 format.**

I. INTRODUCTION

The last decade has seen the continuous growth of communication services [1], and in particular important demand for activities such as remote work, e-learning, e-healthcare and intensification of social relations supported by massive data transmission. This situation gave a new impulse to further investigate various methods to increase optical networks' capacity towards Tb/s/channel objectives.

Advances in optical/electronic technologies as well as in systems with new transmission formats using innovative DSP algorithms allow higher transmission rates and increased spectral efficiency [2]. In this context, multi-level coded transmission and M-ary quadrature amplitude modulation (M-QAM) are of particular interest.

A direct consequence of this trend, in particular the decision to adopt the gigabit Ethernet standard based on four-level pulse amplitude modulation (PAM-4) format, is the need for devices combining very high symbol rate multi-level signal generation with large output swing to efficiently drive electro-optical (E/O) modulators.

Among different challenges for optical transceiver components [2], the E/O modulator and corresponding driver specifications must be properly defined. Modulators are realized in various technologies with a number of trade-offs in their design, like large electro-optical bandwidth (BW), low V_π, and small footprint. Driver design for high speed and high performance transmission also faces a set of conflicting constraints (large electrical bandwidth, high-speed large signal operation, matching modulator input impedance, low power consumption and small footprint).

The most popular optical transmitter architecture consists in cascading high resolution and high-speed DACs with linear drivers, either implemented in a lumped or distributed architecture. Indeed, in [3], a 55-nm SiGe BiCMOS linear driver operating at 64 GBaud PAM-4 with 4.8$V_{pp\ diff}$, is reported. In [4], an indium phosphide (InP) double heterojunction bipolar transistor (DHBT) based linear driver shows a 3-$V_{pp\ diff}$ PAM-4 output swing at 80 GBaud. A linear active combiner realised in SiGe bipolar technology is presented in [5]. This combiner generates 64 GBaud PAM-4 signal with 1.6-V_{pp} differential swing. The 130-nm SiGe BiCMOS distributed linear amplifier [6] presents PAM-4 operation at 45 GBaud with a 4-$V_{pp\ diff}$ output signal. However, it should be noted that a distributed architecture comes with large chip footprint. The efficient alternative transmitter architecture consists in merging DAC and driver functionalities in a single Power-DAC component, as in [7], where the device operates at 100-GBd in PAM-4 mode with a 3.7-$V_{pp\ diff}$ output signal.

In this paper, we present a modulator-driver using 2-bit Power-DAC architecture fabricated in III-V Lab's 0.7-µm InP/GaAsSb DHBT technology. The circuit, named DAC-driver, was designed to provide very high driving swing while operating at high symbol-rates. The circuit design and architecture are presented, as well as the measurement setup. The DAC-driver shows PAM-4 operation at 90-GBd symbol-rate with a record 5.5-$V_{pp\ difff}$ swing, and a 3.35-$V_{pp\ difff}$ swing at 112-GBd.

II. TECHNOLOGICAL PROCESS

Double heterojunction bipolar transistors (DHBTs) allow to extend the breakdown voltage beyond what is possible in single heterojunction transistors, while keeping high frequency performance. InP/GaAsSb DHBTs offer one of the most favourable f_T and f_{MAX} values versus breakdown voltage trade-off, among all bipolar transistors.

The DAC-driver IC is fabricated in III-V Lab 0.7-µm InP DHBT technology [8], using InP/GaAsSb epitaxial structure grown by metalorganic vapour-phase epitaxy (MOVPE) at ETH-Zürich. Details on the epitaxial structure and technological process can be found in [9-11].

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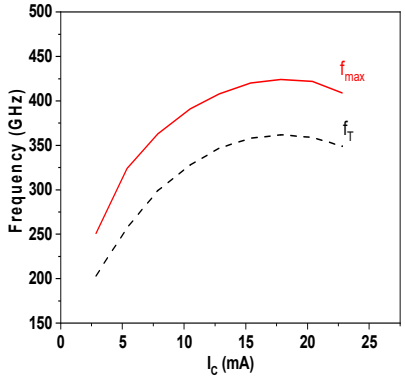
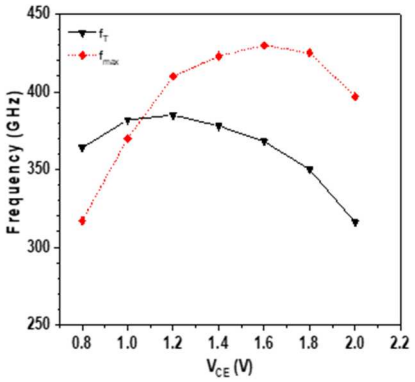
Transistors used in this design have a DC current gain of about 40, an about 4.5-V breakdown voltage, BV_{CE0}, with a large Safe Operating Area (SOA). Peak f_T and f_{MAX} are above 360 and 420 GHz respectively at a collector current density of 6 mA/µm² and a 1.6-V collector-emitter voltage, V_{CE}. In Fig.1, f_T and f_{MAX} performances, for 0.7x5µm²-emitter transistor, are presented. It should be noted that even at lower V_{CE} values, high f_T and f_{MAX} performances are obtained, allowing excellent circuit frequency capabilities with low power consumption. Concerning passive elements, NiCr thin film resistors, Si_3N_4 MIM capacitors and three Au-based interconnect levels are available in the process.



a.



b.

Fig. 1. f_T and f_{MAX} performances of 0.7x5µm²-emitter transistor
a. f_T and f_{MAX} versus Ic at V_{CE}=1.6V
b. f_T and f_{MAX} peak frequencies versus collector-emitter voltage

III. Operation Principles, Architecture and Design

The DAC circuit transforms n binary input data streams into PAM-2^n output signals. Input signals data rate (D) in bit/s, correspond to output signals' symbol-rate in Baud (D_S), hence corresponding transmission rate is nxD b/s. This DAC-driver circuit realizes the DAC and amplification functions of n=2 data signals and produces PAM-4 electrical output. The DAC-driver block diagram is shown in Fig. 2.

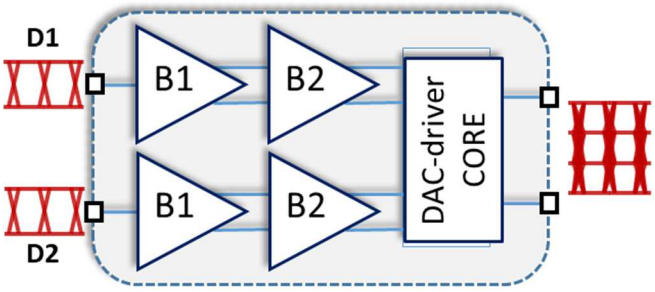


Fig. 2. DAC-driver circuit block diagram

The circuit has two single-ended (SE) inputs corresponding to two binary NRZ data streams. Each data signal is first converted from SE to differential signal (block B1) and pre-amplified (block B2). Both blocks are a cascade of emitter followers and a differential pair to ensure high-speed operation. After these initial operations, the two resulting differential signals are combined and amplified by the circuit core. Blocks B1 and B2 are realized as differential pairs. The first block, B1, uses important passive inductive peaking (L= 80pH) to obtain steep slope binary signals. The amplifying pair B2 has limited peaking to avoid overshoots, however its gain can be controlled by varying the transistor collectors current. This functionality provides adjustable peaking at the DAC-driver's output to compensate, if necessary, E/O modulator's limited bandwidth. The amplifying DAC-driver CORE uses a cascode architecture to relax gain-bandwidth constraints. Two non-return to zero (NRZ) data are combined to obtain a PAM-4 signal with two differential outputs. The standard 2 to 1 ratio is used between MSB (Most Significant Bit) and LSB (Least Significant Bit). However, this ratio can be adjusted through DC controls to obtain predistortion and to compensate for the modulator's nonlinear E/O characteristic; thus preventing the usual driving swing reduction for linear operation and increasing the overall E/O bandwidth. To ensure correct operation on a very large range of symbol rates, no inductive peaking is used in the output block. Large gain control range can be obtained by adjusting the output block's current. Additionally, an output DC offset control allows the optimal electrical signal positioning with respect to the E/O modulator characteristic.

In summary, DC controls allow to adapt the circuit output signals to optimize the overall E/O response: driving swing adjustment, providing static predistortion to compensate for the E/O characteristic nonlinearity, pre-compensating modulator's limited bandwidth and providing necessary DC offset.

The transistor frequency characteristics, shown in Fig. 1, together with DC SOA characteristics are used to determine the optimal position of load cycle thus providing the best trade-off between a large output swing and high-speed operation.

Circuit layout. Input and output signal paths are realized as 50-Ω coplanar lines. DC supplies and controls are decoupled, on-chip, with low ohmic RC-damped decoupling networks. DAC-driver's output signal pads were

implemented with a large pitch for better connectivity with E/O modulators.

A compact layout is privileged to maximally shorten signal connections. Most critical interconnections are identified and their parameters (length, width, metal level and configuration) are chosen to minimise unwanted parasitic effects. Layout symmetry is applied wherever possible to improve common mode rejection. The output cascode block is a critical region, as thermal dissipation needs to be correctly apprehended. The power intensity is high and the heat needs to be safely evacuated. On the other hand, the signal integrity should be preserved and the interconnect dimensions kept under control in order not to limit operation speed. The optimal distance between transistors is hence implemented.

The IC is composed of 37 transistors. The microphotograph of the fabricated circuit die is presented in Fig. 3. The IC footprint is 1.2 x 1.5 mm², while circuit's core dimensions are 520x470 µm².

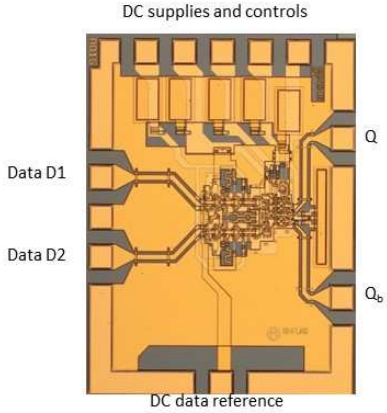


Fig. 3. A die microphotograph of DAC-driver circuit

IV. Measurement Setup and Results

On-wafer measurements are performed in a wide range of bit-rates/symbol-rates. Two single-ended non-return-to-zero (NRZ) signals are provided at the circuit inputs (D1 and D2). The circuit then produces large swing differential PAM-4 outputs (Q and Qb) to directly drive the E/O modulator.

PAM-4 measurements at 90 and 112 GBd are presented. Circuit input eye diagrams at 90 Gb/s are presented in Fig. 4. It should be noted that those measurements include cables, transitions, delay lines and DC blocks, which impact signal integrity. D1 and D2 amplitudes are respectively 362 and 380 mV. Eye heights are 185 and 227 mV respectively.

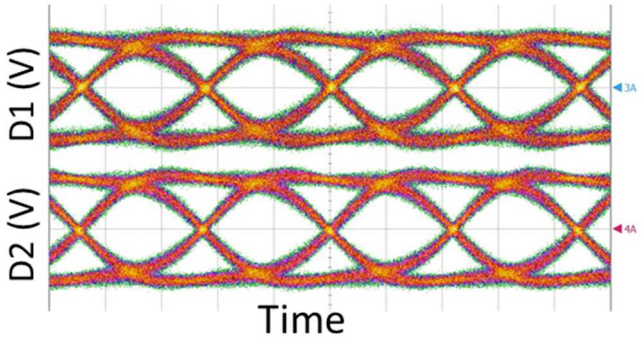


Fig. 4. 90 Gb/s NRZ inputs with 362 and 380-mV amplitude, 420 and 326-fs rms timing jitter. Scale: (200mV/div, 5ps/div)

The circuit's outputs are connected to the oscilloscope's 70-GHz remote sampling heads through 65-GHz 20-dB attenuators. The 90-GBd PAM-4 differential output eye diagram, with a record 5.5-V_{pp} swing and an excellent eye quality, is presented in Fig. 5.

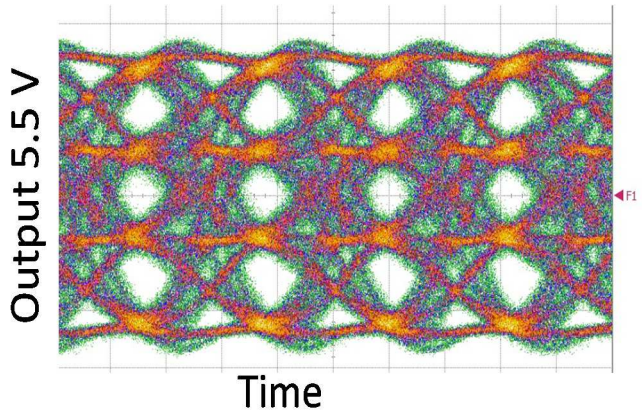


Fig. 5. 90-GBaud (180 Gb/s) PAM-4 differential output eye diagram with 5.5-$V_{pp\ diff}$ output swing. Scale: (1V/div, 5ps/div)

The DAC-driver's gain control capability through dc controls adjustments is shown in Fig. 6. The voltage output swing variation from 1.3 to 5.5 $V_{pp\ diff}$, thus testifies of an about 12-dB gain control dynamic, while maintaining a very high PAM-4 eye quality.

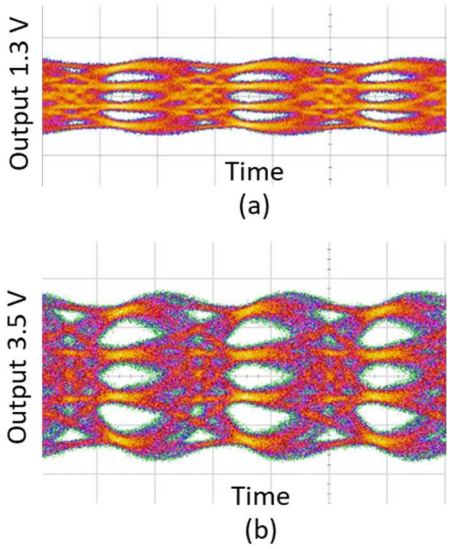


Fig. 6. 90-GBaud PAM-4 measurement with output amplitude tuning (a) 1.3-$V_{pp\ diff}$ (b) 3.5-$V_{pp\ diff}$ Scale: (1V/div, 5ps/div)

The circuit measurement at 112-GBaud PAM-4 is presented in Fig. 7 with a record 3.35-$V_{pp\ diff}$ output swing. It should be noted, that the 112 Gb/s measurement input interface has an important negative impact on the input signal quality.

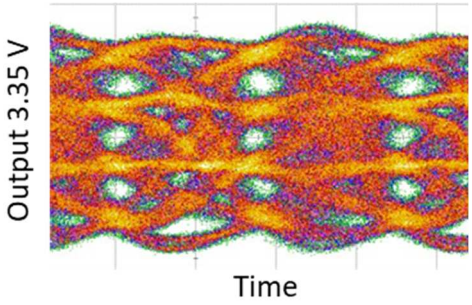


Fig. 7. 112-GBaud PAM-4 measurement with output amplitude 3.35--$V_{pp\ diff}$ Scale: (1V/div, 5ps/div)

Power consumption depends on the output swing and is equal to 1.1 W for a 5.5-$V_{pp\ diff}$ output swing (90 GBd operation) and to 0.6 W for 3.35-$V_{pp\ diff}$ output swing (112 GBd).

The figure-of-merit ([12], modified in [4]) expressing the driving efficiency of E/O modulator driver at a given symbol rate is defined as:

$$FoM = \frac{D_S . V_{out}^2}{8 . Z_0 . P_{DC}}$$

where: D_S - is PAM-4 symbol rate, V_{out} - is the single-ended or differential output swing at a D_S symbol-rate, Z_0 is the single-ended or differential output impedance and P_{DC} is the DC power consumption of the circuit.

This DAC-driver shows record FoM at 90 and 112 GBd of respectively 3.1 and 2.6-GBd.

V. Conclusion

The presented PAM-4 DAC-driver based on 2-bit power-DAC architecture is realized using a 0.7-µm InP/GaAsSb DHBT technology. Main process characteristics and, in particular, transistor frequency performances in function of applied voltage and current are given. The circuit architecture, design and layout trade-offs are presented.

Operating at 90 GBd (180 Gb/s) the circuit achieves a record 5.5-$V_{pp\ difff}$ output swing with excellent PAM-4 eye diagram quality, and a record 3.35-$V_{pp\ difff}$ output swing at 112 GBd (224 Gb/s). Power consumption for these two measurements are 1.1 and 0.6 W respectively. E/O modulator driver figures of merit are 3.1 and 2.3 GBd for these two symbol-rates. A large tuning range of circuit's output amplitude, with limited impact on the PAM-4 eye diagram quality, is shown. The proposed InP DHBT circuit can efficiently drive E/O modulators using very-high-symbol-rate PAM (or QAM) modulation formats. The implemented adjustable predistortion, pre-compensation and output DC offset control capabilities aim at finely optimizing the overall E/O response for future Tb/s/channel optical communication systems.

Acknowledgment

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