100 GBaud DSP-free PAM-4 optical signal generation using an InP-DHBT AMUX-driver and a Thin-Film Lithium Niobate Modulator Assembly

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Abstract—In this article, we report on the generation of 100-GBd (200-Gb/s) 4-level pulse-amplitude modulation (PAM-4) optical signal, without any support of digital signal processing (DSP) nor off-line equalisation. This is achieved in using an uncooled indium phosphide (InP) analog-multiplexer (AMUX)-driver and a thin film lithium niobate (TFLN) Mach-Zehnder modulator (MZM) assembly, with a -3-dB electro-optical bandwidth in excess of 85 GHz. This result paves the way for low-power DSP-free beyond-1-Tb/s transceivers for next generation optical communication systems and 6G applications. We also present the design and characterisation of the AMUX-driver integrated circuit (IC). The InP-DHBT IC shows a 2-Vppd output swing at 100 GBd in PAM-4 while operating at a 100-GSa/s sampling-rate.

Index Terms—Analog-multiplexer, large-swing linear modulator driver, Mach-Zehnder modulator, high-speed analog integrated circuits, Tb/s optical communications, Indium Phosphide (InP) double heterojunction bipolar transistor (DHBT), thin film lithium niobate (TFLN), 4-level pulse amplitude modulation (PAM-4)

I. Introduction

The hyperbolic scaling of transmitted data volume together with bandwidth and power hungry applications (artificial intelligence, cloud computing, video streaming, *etc.*) stress the need for low environmental imprint and high-capacity communication systems, [1]. This necessitates high-performance and low-power transceivers, with limited DSP and active cooling usage. To meet this challenge, a careful selection of materials for the design of electronics and photonics ICs is key.

InP technologies are gaining traction as strong candidate for the development of high-power and low-noise advanced-5G and 6G transceivers [2], thus requiring high-volume and low-cost productions. This could trigger growing financing and development towards their integration on silicon [3], paving the way towards InP technologies adoption in the industry. Besides, TFLN modulators broad-bandwidth and low-driving-voltage (V π), [4], are very promising to achieve high-performance low-power-consumption transceivers [5], while being compatible with silicon photonics.

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Using an analog-multiplexer, 100-GBd-and-beyond optical signals have been reported in [6], [7], yet with heavy DSP usage to compensate for the device impairments (limited bandwidth, non-linearity, *etc.*). In this article, we report on the generation of 100-GBd DSP-free PAM-4 optical signals using an uncooled InP-DHBT AMUX-driver and TFLN MZM assembly with a -3-dB small-signal E/O bandwidth of 85.2 GHz. Section II presents the AMUX-driver IC design and measurements, with a detailed discussion on the interleaving cell load impact on the performance. Section III describes the AMUX-driver/MZM assembly preparation, characterisation setup and discusses the results. Section IV concludes this article.

II. INP DHBT AMUX-DRIVER IC

A. AMUX Interleaving cell design

In [7]–[9], it has been shown that InP-DHBT AMUXs can conjugate very-high sampling-rate operation and large output swing. Such AMUX interleaving cell schematic is depicted on Fig.1(a). While its design is largely discussed in the literature, the impact of its load on the performance is yet not really addressed. This section shows how critical the load is to ensure very-high performances, especially when considering the AMUX and the linear modulator driver monolithic integration.

In [7], [9], [10], the interleaving cell output is resistively loaded (RES) [see nodes $X_{\text{N/P}}$ on Fig.1(a) and 1(b)], yielding low-complexity designs. In [11], [12], a cascode load [see Fig.1(c)] is employed to boost the bandwidth. In [14], a regulated cascode load is used to improve the interleaving cell's bandwidth while preserving linearity, yet the impact of a regulated cascode on linearity is not detailed in [14].

In Fig.2(a), the interleaving cell simulated small-signal voltage gain is compared for different load designs. For this comparison, the entire tail current, I_{ee} , is flowing through (Q1/Q3-Q4) in forcing $V_{BEQ1} >> V_{BEQ2}$ with a DC reference on Q1-Q2 bases. This mimics the sampling state of the interleaving cell and is later referred to as "path-through mode". Note that emitter followers have been used at the interleaving cell's inputs and after the loads, for impedance matching on 50 Ω . Although the CS provides significant bandwidth extension compared to the RES, it however slightly reduces the low-frequency gain and tends to degrade linearity. Indeed, in Fig.2(b) the simulated *rms*-THD versus the output swing is compared for different loads, respectively at 1 and 30 GHz excitation frequencies. The input signals are applied on Q3-Q4

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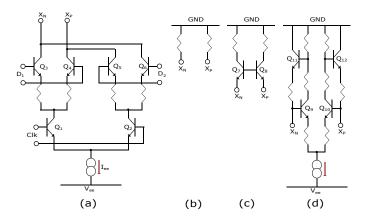


Fig. 1. (a) AMUX interleaving cell schematic with different load designs. (b) Resistive load (RES). (c) Cascode load (CS). (d) Transimpedance load (TIS)

input paths and the interleaving cell is operated in the paththrough mode. Hence, the resistive and the cascode loads do not conjugate high bandwidth with high linearity and output swing. Additional amplifying stages may then be required before the driver stage, and force extra emitter followers to be used, at the expanse of footprint, signal integrity and power consumption.

The schematic of a transimpedance stage (TIS) load with active feedback (see [15]) is presented in Fig.1(d). Using a TIS to load a transadmittance stage, i.e. the interleaving cell in this case, reduces the capacitance seen at nodes $X_{N/P}$, thanks to the feedback. It results in a significant bandwidth extension while the low-frequency gain can also be increased. Indeed, as shown on Fig.2(a), the gain-bandwidth product of the TIS implementation is 50% higher than with the CS load. Additionally, as shown on Fig.2(b), the TIS load active feedback also significantly improves the interleaving cell's linearity and output swing. Indeed, at 1 GHz and 1% of rms-THD, the TIS achieves an about 50% higher output swing compared to the resistive and cascode implementations. Hence, the TIS architecture has strong advantages with respect to the AMUX and modulator driver monolithic integration, as no additional amplification is required before the output stage.

B. InP-DHBT AMUX-driver design and characterisation

The AMUX-driver is designed with a lumped architecture to minimize footprint, and broadband coplanar waveguides for a high bandwidth. Single-ended input interfaces, located on the same facet, and on-chip R-C-damped decoupling networks are used to ease packaging efforts. Input amplifiers act as active baluns for single-ended to differential conversion. An interleaving cell with a TIS load is implemented, to maximize bandwidth, sampling-rate, linearity and output swing, see section II-A. It drives the large-swing output stage through emitter followers to maximize the overall bandwidth, while saving $\approx\!10\%$ in power consumption compared to [8]. The output stage is based on a paralleled-transistor cascode architecture with resistive degeneration, see [16], [17], to allow a direct drive of the E/O modulator, without additional external amplifier.

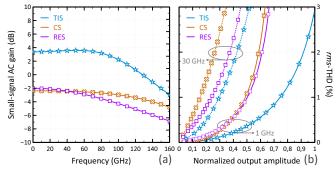


Fig. 2. Path-through-mode AMUX interleaving cell simulated performances' comparison for different load designs. (a) Small-signal AC gain. (b) root-mean-square total harmonic distortion (*rms-THD*) versus the normalized output voltage swing. Results are displayed with solid lines for a 1-GHz excitation frequency and dotted lines for a 30-GHz excitation frequency. The output swing is normalized to the TIS implementation output swing when it reaches 3% of *rms-THD* at 1 GHz.

Legend: magenta curves with squares correspond to the resistive load (RES), gold curves with crosses to the cascode load (CS) and blue curves with stars to the transimpedance load (TIS)

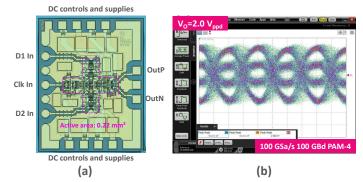


Fig. 3. InP DHBT AMUX-driver (a) die microphotograph. (b) large-signal 100-GBd (200-Gb/s) PAM-4 differential output eye diagram measurement. Horizontal and vertical scales are 5 ps/div and 400 mV/div, respectively

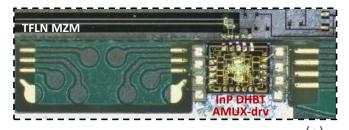
The AMUX-driver IC micro-photograph is depicted on Fig.3(a). It was fabricated in III-V Lab in-house 0.5- μ m InP DHBT technology which features a 45 static-current gain, β , a 4-V breakdown voltage, BV_{CE0}, and 360-/450-GHz f_T/f_{MAX} , see [16], [18] for more information on the process. The die measures 1.2×1.5 mm², with a 0.22-mm² active core area. At a 2-Vppd output swing the AMUX-driver total DC power consumption is 1.2 W. The main V_{EE} source was set to -4.1 V.

On-wafer large-signal characterisation was performed on the AMUX-driver IC at 100 GBd in PAM-4 (200 Gb/s). The resulting electrical output eye diagram is depicted on Fig.3(b), showing clear eye opening with a 2-Vppd output swing, while the IC operates at a 100-GSa/s sampling-rate. Note that no DSP or off-line equalisation was used. The setup is similar to [8], using an in-house module as PAM-4 source and a 122-GHz equivalent time sampling oscilloscope, see section III-B.

III. ULTRA-HIGH-BANDWIDTH E/O ASSEMBLY

A. Assembly description and characterisation setup

After wafer dicing, the AMUX-driver chip has been assembled on a PCB with a MZM, using $50\times220~\mu m$ wire-bond, as depicted on Fig.4(a). The modulator has been realised on the



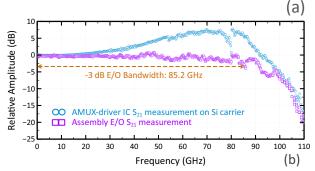


Fig. 4. (a) AMUX-driver/MZM assembly microphotograph. (b) AMUX-driver IC S_{21} measured on a 1-mm-thick silicon carrier (blue circles) and Assembly small-signal electro-optical bandwidth measurement (magenta squares)

TFLN platform from Liobate, [4], and measures 22.5 mm. It exhibits an about 1-V $V\pi$, determined using a 10-GHz sinusoidal RF signal, and a 64-GHz electro-optical -3-dB bandwidth. The modulator was specifically designed for this assembly to limit packaging efforts and interconnection losses. All PCB design and assembly steps were performed at III-V Lab. The PCB accommodates the chips' heights to minimise wire-bond length and preserve high-frequency performances, as well as R-C-damped decoupling network for biasing. The modulator is driven single-ended and terminated on chip. The AMUX-driver unused output is loaded with a resistance on the modulator chip, see Fig.4(a).

Using a 2-port *Anritsu* ME7838A vector network analyzer (VNA) with a 3739A frequency extender and a 110-GHz calibrated photodiode, the electro-optical small-signal response of the assembly has been measured up to 110 GHz. During this measurement, the AMUX-driver is operated in the path-through mode. After removing the input probe and photodiode contributions, an 85.2-GHz -3-dB E/O bandwidth is obtained for the AMUX-driver/MZM assembly, see Fig.4(b). The roll-off is rather smooth up to the -6 dB bandwidth, at 100 GHz. This very-high electro-optical bandwidth is obtained thanks to the AMUX-driver gain peaking (7.8 dB at 80 GHz), see Fig. 4(b), which compensates for the high-frequency interconnection and modulator losses, as explained in [8], [16], along with a careful assembly process. Note that the standalone AMUX-driver IC bandwidth is 97 GHz.

B. Large-signal measurements and discussion

The assembly large-signal electro-optical performance was assessed using the setup depicted on Fig.5. A *Wiltron* 69177A 70-GHz frequency synthesizer is used to generate a 50-GHz clock signal. This signal is amplified to drive the AMUX-driver, the *Agilent* DCA-X 86100D equivalent time sampling oscilloscope precision time-base and the *SHF* 12100B bit

pattern generator. The last provides a trigger signal for the oscilloscope and is used to generate 50 Gb/s PRBS non-returnto-zero (NRZ) signals. A V-connector delay line de-correlates these 50 Gb/s signals to be combined into 50 GBd PAM-4, using an in-house InP-DHBT 2-bit active combiner module, see [19]. NRZ signals can also be generated in disabling one bit in the combiner's output stage. After the combiner, another V-connector delay-line de-correlates "D2" from "D1" to drive the AMUX-driver, while allowing to manually adjust their relative time positioning for optimal interleaving. The AMUXdriver input clock phase is also manually adjusted through a delay line. The input signals (D1, D2 and Clk) are provided to the AMUX-driver through V-to-W adapters and a 110-GHz W-connector probe. An external tunable laser source is connected to the modulator input providing 12 dBm optical power at 1560 nm. An erbium-doped fiber amplifier (EDFA) amplifies the modulated optical output signal. At the receiver side, a 110-GHz-bandwidth U^2t XPDV 4120R photodiode is connected to the 122-GHz bandwidth oscilloscope remote head for signal acquisition. The photodiode current was 4 mA. In this experiment, no active devices were used for cooling or thermal management, the modulator is driven at 0.9-Vpp and the AMUX-driver operates at a 100-GSa/s sampling-rate.

The 100-GBd NRZ and PAM-4 optical received eye diagrams are respectively depicted on Fig.6(a) and 6(b). The 100-Gb/s NRZ eye diagram shows a 7-dB extinction ratio with clear eye opening. On Fig.6(b), the PAM-4 levels can clearly be distinguished, yet some noise is observed. This is first due to a limited optical power, which was insufficient to operate the EDFA in the saturation regime, and secondly due to the absence of optical filter in front of the photodiode. Note that PAM-4 eye-diagram measurement was not available on the oscilloscope and that bit error rate (BER) measurement could not be conducted at 100 GBd due to the lack of necessary equipment. It should be noted that no DSP or offline equalisation was used during this experiment, the obtained results hence directly reflect the E/O assembly plus setup performances. This shows the feasibility of DSP-free uncooled optical 100-GBd PAM-4 generation. These results could be further improved in using a higher output-power laser source and/or an optical filter to reduce noise at the receiver.

IV. CONCLUSION

This article reports on an 85.2-GHz bandwidth InP-DHBT AMUX-driver and TFLN modulator assembly. We demonstrate the feasibility of 100-GBd NRZ and PAM-4 optical signal generation without active cooling, nor any support of DSP nor off-line equalisation. This paves the way for next generation low-power Tb/s transceivers thanks to high-performance and high-efficiency ICs. We also show that AMUXs' bandwidth, linearity and output swing can be significantly improved with a transimpedance stage load in the interleaving cell, which facilitate the monolithic integration with the modulator driver.

REFERENCES

[1] Cisco, "Cisco Annual Internet Report (2018-2023) White Paper". cisco.com. Accessed: Jan. 5, 2023 [Online.] Available: https:

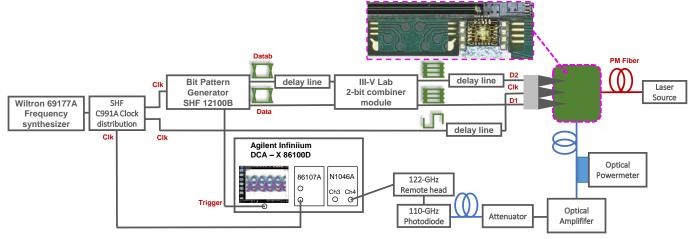


Fig. 5. InP DHBT AMUX-driver/ TFLN MZM assembly large-signal electro-optical characterisation setup schematic

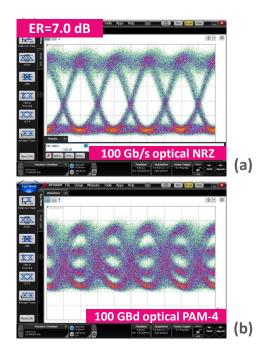


Fig. 6. AMUX-driver/MZM assembly optical eye diagram measurements. (a) 100-Gb/s NRZ optical signal with a 7-dB extinction ratio. (b) 100-GBd (200-Gb/s) PAM-4 optical signal. Horizontal axis scales are 5 ps/div.

//www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.pdf.

- [2] B. Debaillie et al., "European Core Technologies for future connectivity systems and components: D3.3 Initial COREnect industry roadmap". COREnect.eu, Accessed: Aug. 5, 2022, [Online.] Available: https://www. corenect.eu/publications.
- [3] M. Urteaga et al., "THz bandwidth InP HBT technologies and heterogeneous integration with Si CMOS," 2016 IEEE Bipolar/BiCMOS Circuits and Technol. Meeting (BCTM), 2016, pp. 35-41, doi: 10.1109/BCTM.2016.7738973
- [4] M. Xu et al., "Dual-polarization thin-film lithium niobate in-phase quadrature modulators for terabit-per-second transmission," Optica 9, 61-62 (2022), doi: 10.1364/OPTICA.449691
- [5] S. Almonacil et al., "260-GBaud Single-Wavelength Coherent Transmission over 100-km SSMF based on Novel Arbitrary Waveform Generator and Thin-Film Niobate I/Q Modulator," in J. of Lightwave Technol., doi: 10.1109/JLT.2023.3269740
- [6] Q. Hu et al., "120 GSa/s BiCMOS AMUX for 360 Gbit/s High-Information-Rate Signal Generation Demonstrated in 10 km IM/DD System," in J. of Lightwave Technol., vol. 40, no. 5, pp. 1330-1338, 1

- March1, 2022, doi: 10.1109/JLT.2021.3133409
- [7] M. Nagatani et al., "A Beyond-1-Tb/s Coherent Optical Transmitter Front-End Based on 110-GHz-Bandwidth 2:1 Analog Multiplexer in 250nm InP DHBT," in IEEE J. of Solid-State Circuits, vol. 55, no. 9, pp. 2301-2315, Sept. 2020, doi: 10.1109/JSSC.2020.2989579.
- [8] R. Hersent et al., "160-GSa/s-and-Beyond 108-GHz-Bandwidth Over-2-Vppd Output-Swing 0.5-µm InP DHBT 2:1 AMUX-Driver for Next-Generation Optical Communications," in IEEE Microwave and Wireless Components Letters, vol. 32, no. 6, pp. 752-755, June 2022, doi: 10.1109/LMWC.2022.3161706.
- [9] R. Hersent et al., "Analog-Multiplexer (AMUX) circuit realized in InP DHBT Technol. for high order electrical modulation formats (PAM-4, PAM-8)," 2020 23rd Int. Microwave and Radar Conference (MIKON), 2020, doi: 10.23919/MIKON48703.2020.9253772
- [10] D. Ferenci, M. Grozing and M. Berroth, "A 25 GHz Analog Multiplexer for a 50GS/s D/A-Conversion System in InP DHBT Technology," 2011 IEEE Compound Semiconductor Integrated Circuit Symp. (CSICS), 2011, doi: 10.1109/CSICS.2011.6062440
- [11] T. Tannert et al., "A SiGe-HBT 2:1 analog multiplexer with more than 67 GHz bandwidth", 2017 IEEE Bipolar/BiCMOS Circuits and Technol. Meeting (BCTM), 2017, doi: 10.1109/BCTM.2017.8112931
- [12] M. Collisi and M. Möller, "A 120 GS/s 2:1 Analog Multiplexer with High Linearity in SiGe-BiCMOS Technology," 2020 IEEE BCIT Symp. Proc., Monterey, USA, 2020, doi: 10.1109/BCICTS48439.2020.9392970
- [13] T. Tannert et al., "Analog 2:1 Multiplexer with over 110 GHz Bandwidth in SiGe BiCMOS Technology," 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technol. Symp. (BCICTS), 2021, doi: 10.1109/BCICTS50416.2021.9682492
- [14] H. Ramon et al., "A 100-GS/s Four-to-One Analog Time Interleaver in 55-nm SiGe BiCMOS", in IEEE J. of Solid-State Circuits, vol. 56, no. 8, pp. 2539-2549, Aug. 2021, doi: 10.1109/JSSC.2021.3057575.
- [15] C. D. Holdenried, J. W. Haslett and M. W. Lynch, "Analysis and design of HBT Cherry-Hooper amplifiers with emitter-follower feedback for optical communications," in *IEEE J. of Solid-State Circuits*, vol. 39, no. 11, pp. 1959-1967, Nov. 2004, doi: 10.1109/JSSC.2004.835819.
- [16] R. Hersent et al., "InP DHBT linear modulator driver with a 3-Vppd PAM-4 output swing at 90 GBaud: from enhanced transistor modelling to integrated circuit design" in *IEEE Trans. on Microwave Theory and Techn.*, doi: 10.1109/TMTT.2023.3305150
- [17] H. Romain et al., "Over 70-GHz 4.9-Vppdiff InP linear driver for next generation coherent optical communications," 2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technol. Symp. (BCICTS), 2019, doi: 10.1109/BCICTS45179.2019.8972779
- [18] V. Nodjiadjim et al., "0.7-μm InP DHBT Technology with 400-GHz f_T and f_{MAX} and 4.5-V BVCE0 for High Speed and High Frequency Integrated Circuits," in IEEE J. of the Electron Devices Society, 2019, doi: 10.1109/JEDS.2019.2928271
- [19] A. Konczykowska et al., "112 GBaud (224 Gb/s) large output swing InP DHBT PAM-4 DAC-driver," 2022 24th Int. Microwave and Radar Conference (MIKON), 2022, pp. 1-4, doi: 10.23919/MIKON54314.2022.9924653