0.4-µm InP/InGaAs DHBT with a 380-GHz f_T, > 600-GHz f_{MAX} and BV_{CE0} > 4.5 V

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***Abstract*—We report on a 0.4-µm emitter width composition-graded-base InP/InGaAs/InP DHBT technology featuring a current gain cutoff frequency (f_T) and a maximum oscillation frequency (f_{MAX}) of 380 GHz and 605 GHz, respectively. The DHBTs demonstrate a maximum static current gain of 29 and a common-emitter breakdown voltage of 4.7 V. RF performances above 600 GHz were achieved through emitter size scaling and base contact width shrinking. Further investigations on measurements were performed by comparing three VNA calibration methods as well as through extraction of small-signal parameters over the 110 GHz measurement range.**

Keywords*—Double heterojunction bipolar transistor (DHBT), maximum oscillation frequency (f_{max}), Characterization, InP/InGaAs, millimeter-wave

I. Introduction

To meet the growing demand of THz-range systems, be it for wireless communication, optical transmission or for imaging, various ultra-high-speed transistor technologies have emerged. InP heterojunction bipolar transistor (HBT are strong contenders for this competition. This technology has the potential to reach THz frequencies while combining high linearity and high breakdown voltage. InP/InGaAs/InP type-I DHBT have already been studied widely. Aggressive scaling of the emitter width has led to f_{MAX} > 1 THz as shown in [1] and [2] with a breakdown voltage (BV_{CE0}) of 3.5 V. These performances have been achieved through engineering of the type-I base-collector heterojunction to improve both high frequency performances and high breakdown voltages. However, improving HBT performances through scaling is challenging as it increases the thermal resistance, which, in turn, negatively impacts the transistor performances, and decreases the breakdown voltage following collector thickness reduction.

In this paper we report 0.4 × 5 µm² InP/InGaAs DHBTs exhibiting f_{MAX} = 605 GHz and f_T = 380 GHz. The device shows a peak current gain of 29 and a common emitter breakdown voltage of 4.7 V. The improvement of RF performances is due to the reduction of the base-collector capacitance achieved through emitter size scaling and base contact width shrinking. The rest of this paper is organized as follows: section II details the device architecture and the fabrication process; section III includes device characterization results and small signal modeling, followed by the conclusion.

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II. Device structure and fabrication process

A. Epitaxial structure

The DHBT structure was grown on a 3-inch semi-insulated InP substrate by IntelliEPI using solid source molecular beam epitaxy. The current scheme of epitaxy is an optimized version of the one introduced in [3]. The emitter contact is formed with highly n-doped $In_{0.85}Ga_{0.15}As$ in order to have a low emitter contact resistance. The structure consists of a 40-nm InP emitter Si-doped at 5×10^{17} cm^{-3}. The 28-nm thick $In_xGa_{1-x}As$ base is compositionally graded from x = 0.47 at the emitter side to x = 0.53 at the collector side. This grading in composition induces a 40-meV conduction band slope across the base that reduces the transit time. In order to minimize the base sheet resistance, the base layer is heavily C-doped (8×10^{19} cm^{-3}) without doping grading. A base sheet resistance of 730 Ω/□ is extracted from transmission line measurements. A 130-nm thick composite collector is used. It is composed of an InGaAs unintentionally doped spacer, a 25-nm thick heavily doped InP region (4×10^{17} cm^{-3}) and a lightly doped InP layer (1.5×10^{16} cm^{-3}). This low doping concentration has been chosen to keep a high breakdown voltage. A 5-nm heavily n-doped $In_{0.53}Ga_{0.47}As$ layer is used as sub-collector. It allows a low thermal resistance while keeping a satisfying collector contact resistance.

B. Fabrication process

The 0.4 µm emitter width DHBTs are processed using a wet-etch self-aligned triple mesa technology. A base contact width (W_B) of 0.2 µm is chosen to extends on each side of the emitter. The tasks that require high alignment accuracy like the emitter contact, the base contact and the base plug are processed using e-beam lithography. The other steps are processed using stepper lithography. The contacts are formed with Ti/Pd/Au stacks using vacuum evaporation. The first step consists of emitter contact deposition and emitter mesa etching. Under etching of the emitter results in an effective emitter width W_E = 0.36 µm which has subsequently been taken into account for the calculation of all current densities. Then, the base contact is deposited followed by SiN encapsulation (which improve yield and reliability) and base mesa wet etching. Afterwards, the collector metallization is performed along with the base and the collector plugs followed by the collector mesa etching. Fig. 1 shows an scanning electron microscopy (SEM) view of a transistor after this etching step.

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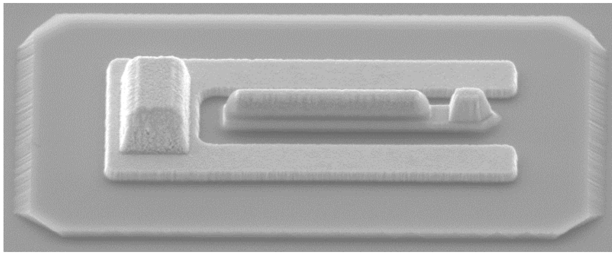

Fig. 1 SEM image of a 0.4 × 5 µm² DHBT after collector mesa etching

Finally, the device is fully encapsulated with SiN and planarized with polyimide. The final step consists of the polyimide etching to form the interconnections of the device. The transistor fabrication yield is above 98% which is sufficiently high to consider using these devices for future realization of medium-scaled integrated circuits.

III. Device Characteristics

A. Measurement procedure

The RF measurements were performed from 250 MHz to 110 GHz with an Anritsu VectorStar network analyzer and 100-µm pitch Picroprobe RF probes. The pad parasitic elements were de-embedded using on-wafer open and short standards. Difficulties in extracting the Mason's unilateral power gain U led to further investigations on the calibration methods. Three calibration methods have been used: the Short-Open-Load-Thru (SOLT), the Advanced Line-Reflect-Match (ALRM) and the multiline Thru-Reflect-Line [4] (mTRL). All of them have been performed with off-wafer impedance standards. ALRM (also called LRM+) is a modified version of the LRM calibration method where an arbitrary known load is used. SOLT and ALRM require the same standards while mTRL requires other standards plus an additional one to cover the frequency range.

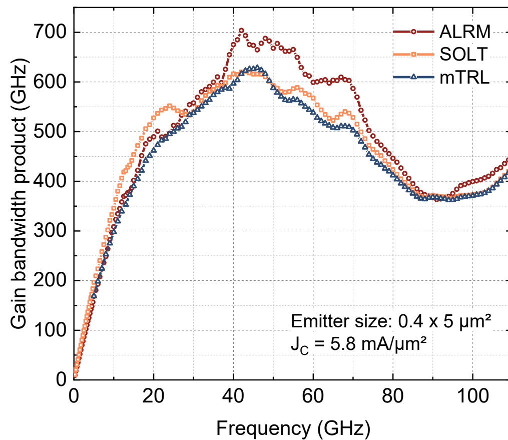

Fig. 2 Mason's gain bandwidth product as function of the frequency for the three studied calibration methods

The gain bandwidth product for the Mason's gain is plotted in Fig. 2 for the three studied calibration methods showing almost identical results up to 40 GHz, and then the ALRM results deviate from the other and overestimates the Mason's gain. Interestingly SOLT and mTRL give very close results. Even though often criticized for its validity for high frequency measurement the SOLT method has been chosen for the rest of the RF characterization. This is particularly because of the fact that this method requires a less number of standards than mTRL, the distance between probes does not need to be changed during calibration and that the validity of this method has already been affirmed up to 200GHz [5]. Another important observation from Fig. 2 is that the gain-bandwidth product starts to collapse after 60-70 GHz for the three methods. A four step de-embedding (pad open, pad short, open, short), that allows to remove the coupling between probes and adjacent structures has also been tested which shows no impact on the curve's shape. Considering these observations, the collapse of the gain-bandwidth product can be attributed to the measurement environment, especially to the coupling between probes and structures. This phenomenon has been demonstrated for 100-µm pitch Picropobe in [6] through EM simulations and is attributed to the crosstalk between port-1 and port-2 probes induced by the probes' design.

B. DC characterization

Fig. 3 shows the Gummel plots at $V_{BC} = 0$ V of a 0.4 × 5 µm² DHBT showing a maximum static current gain of 29 at a collector current density J_C of 4.6 mA/µm². It is a reasonable value considering the base thickness (28 nm) and high doping level (8×10^{19} cm^{-3}). The base and collector ideality factor have been extracted to be $n_B = 1.9$ and $n_C = 1.15$. The deviation of the collector ideality factor from unity is due to the type-I base-collector heterojunction.

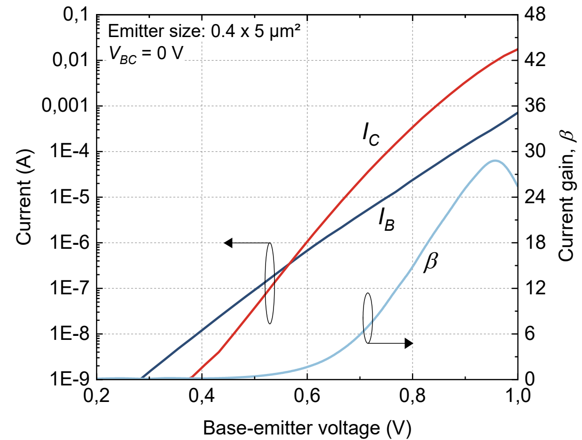

Fig. 3 Gummel plot and DC gain at $V_{BC} = 0$ V of a 0.4 × 5 µm² DHBT.

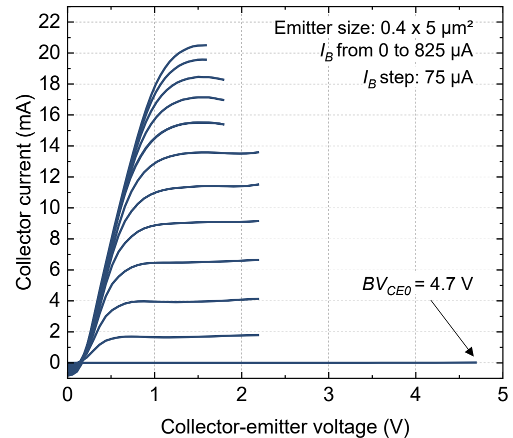

Fig. 4 Common-emitter I_C-V_{CE} curves of a fabricated 0.4 × 5 µm² DHBT.

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The Fig. 4 shows the common-emitter I_C-V_{CE} characteristics for a base current ranging from 0 to 825 µA with 75 µA steps. The common-emitter breakdown voltage BV_{CE0} is 4.7 V at a collector current density $J_C = 0.01$ mA/µm². This breakdown voltage value is obtained thanks to the composite collector optimization. The transistor exhibits a turn-on offset voltage $V_{CE,off}$ of 200 mV.

C. RF characterization

As detailed in part A of this section, describing the RF characterization setup, Fig. 5 shows the short-circuit current gain, h_{21}, and Mason's unilateral power gain, U.

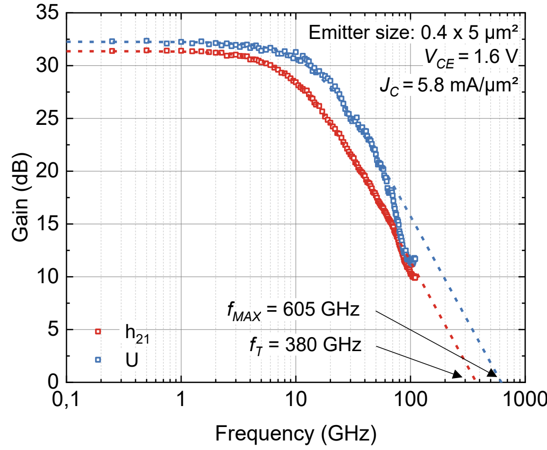

Fig. 5 Short-circuit current gain h_{21} and Mason's unilateral power gain U measured at $V_{CE} = 1.6$ V and $J_C = 5.8$ mA/µm²

The extraction of f_T and f_{MAX} is performed using a single pole transfer function by fitting it against the measurement data up to 70 GHz. As discussed previously, the coupling between probes indeed disturbs the measurements at higher frequencies. This extraction on a 0.4 × 5 µm² DHBT leads to an $f_{MAX} = 605$ GHz and an $f_T = 380$ GHz at $V_{CE} = 1.6$ V and $J_C = 5.8$ mA/µm². The V_{CE} value of 1.6 V is chosen since it gives the maximum value of f_T. This $W_E = 0.4$ µm DHBT technology has been designed to reach the highest f_{MAX} possible with our epitaxial structure. For further analysis, the relationship between f_T and f_{MAX} [7], given by equation (1), has been considered.

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi(R_B C_{BC})_{eff}}} \quad (1)$$

With $(R_B C_{BC})_{eff} = R_{Bx}(C_{BCx} + C_{BCi}) + R_{Bi}C_{BCi}$

To reach a 600 GHz f_{MAX}, efforts were focused on reducing the product $(R_B C_{BC})_{eff}$ in the denominator of (1), especially for reducing C_{BCx} and C_{BCi}. To achieve this the emitter width has been shrinked down to 0.4 µm and the width of the base contact on each side of the emitter has been reduced to $W_B = 0.2$ µm. By shrinking the base contact the value of R_{Bx} is slightly increased, but the total RC product is reduced (in comparison with larger W_B). This effect has already been studied in [8]. Once again, our results highlights the importance of finding the right compromise between R_B and C_{BC}.

The RF figures of merit (f_T and f_{MAX}) of the transistor have been extracted at different collector currents I_C and different collector-emitter voltages, V_{CE}. Fig. 6 shows the results of this extraction. As explained before the maximum of f_T is reached at $V_{CE} = 1.6$ V, whereas, the maximum of f_{MAX} (610 GHz) is reached at a higher voltage $V_{CE} = 1.8$ V. This figures particularly highlight the fact that higher values of f_T and f_{MAX} (>75% of their maximum) can be reached with a wide range of the V_{CE}. This illustrates the interest of this technology for monolithic microwave and high-speed integrated circuits. Circuit designers hence have a wide range of biasing points to exploit the transistor's performances.

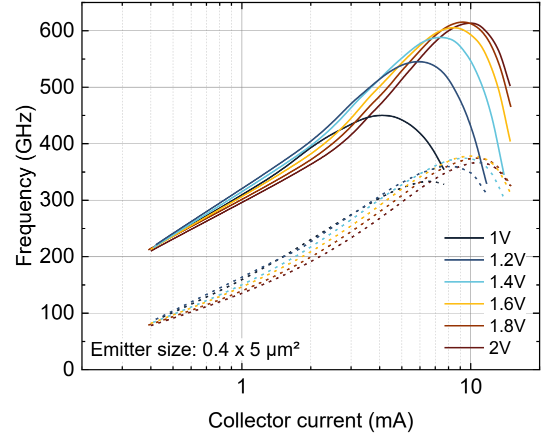

Fig. 6 f_T (dashed lines) and f_{MAX} (solid lines) as function of the current I_C for different V_{CE} values

D. Small-signal modeling up to 110 GHz

The extraction of the small-signal hybrid-π model [9] parameters has been performed on the measurements presented in the preceding section at the peak of f_T i.e. at $V_{CE} = 1.6$ V and $J_C = 5.8$mA/µm². Fig. 7 shows the results of this extraction. A good agreement between measurement and simulation is found at lower frequencies. However, some discrepancies start to appear at higher frequencies. This behavior is conforming to the deviation observed on the Mason's gain beyond 60 GHz which is also present in the measured S-parameters.

Extraction of the small-signal model is often performed at low frequency (< 30 GHz) for different reasons, especially because it is the cleanest part of the measurement. To understand the high-frequency discrepancies extraction of different parameters over the whole frequency range (250 MHz-110 GHz) has been performed. As the discrepancies are mainly observed in the Mason's gain, two parameters are of particular interest: the extrinsic base resistance R_{Bx} and the total base-collector capacitance C_{BC}. Fig. 8 shows the extracted parameters up to 110 GHz. Ideally, these two parameters remain constant over the whole frequency range. However, the extrinsic base resistance shows significant variations over the frequency range. As expected these variations can be directly linked to the behavior of the gain bandwidth products (increase of R_{Bx} results in a decrease of the gain bandwidth product, see part A). Interestingly, this parameter makes it easier to identify the range of validity of the measurements: the frequency at which the value of R_{Bx} is no longer constant is the limit beyond which the measurements are no longer valid. Our measurements are not therefore useful for frequencies higher than 70 GHz.

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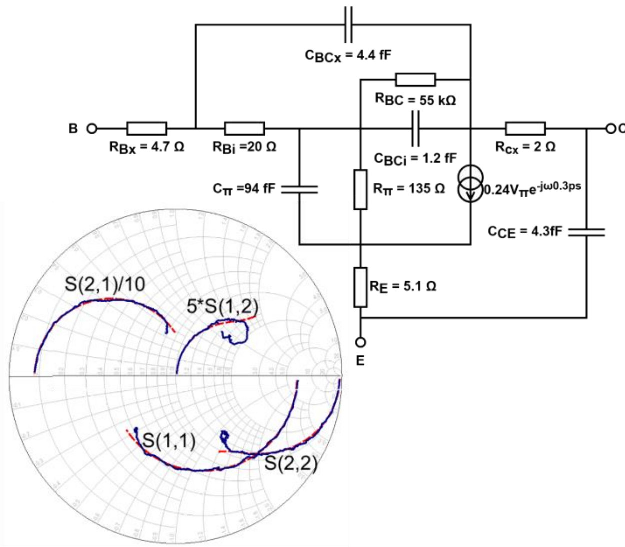

Fig. 7 Hybrid-pi small-signal model of a 0.4 × 5 µm² transistor at V_{CE} = 1.6 V and J_C = 5.8 mA/µm². Comparison between measurement (blue) and simulation (red) is also plotted on the smith-chart.

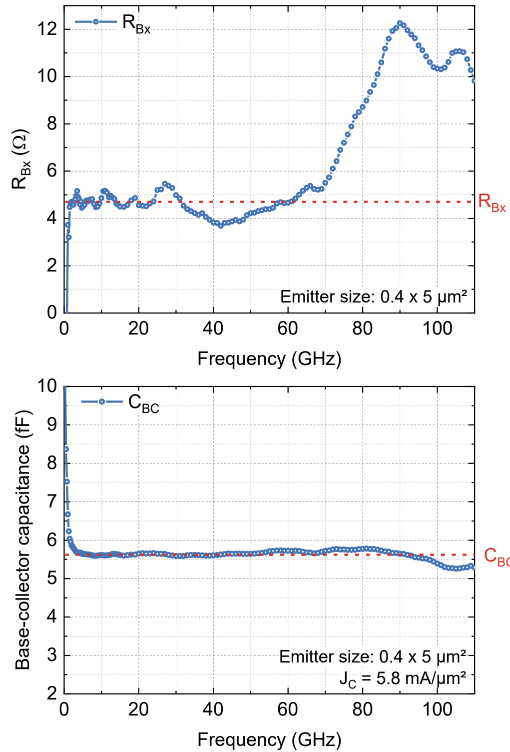

Fig. 8 Extrinsic base resistance R_{Bx} (top) and Base-collector capacitance C_{BC} (bottom) as function of the frequency. Red dash lines indicate the extracted values used in the small-signal model simulation.

The extracted value of C_{BC}, on the other hand, is constant over the whole frequency range and does not indicate any sign of the coupling. The same parameter extraction process can be applied to extract other parameters such as emitter-base capacitance and transit time that are expected to remain constant over the measured frequency range. However, similar to C_{BC}, not all of these parameters might show coupling effects that limit the usable frequency band.

IV. Conclusion and perspectives

We reported a 0.4 × 5 µm² InP/InGaAs DHBT technology with simultaneous cutoff frequencies f_T/f_{MAX} = 380/605 GHz. The device exhibits a peak current gain of 29 and a common emitter breakdown voltage BV_{CE0} = 4.7 V. Comparison between different VNA calibration methods allowed us to choose the most appropriate method. Small-signal model simulation was performed that shows good agreement with measurements. Extraction of small-signal model parameters up to 110 GHz has allowed identifying a simple method to verify the range of measurement validity.

This 0.4-µm DHBT technology demonstrates very high f_{MAX} for a Type-I device without any aggressive emitter scaling. In order to improve f_T while maintaining f_{MAX}>f_T, ongoing work focuses not only on vertical structure optimization thanks to multiscale physical simulations [10] but also on novel tungsten-based emitter process.

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