Analog-Multiplexer (AMUX) circuit realized in InP DHBT technology for high order electrical modulation formats (PAM-4, PAM-8)

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Abstract

Analog-Multiplexers (AMUXs) are attractive architectures to increase electro-optical transmitters' analog bandwidth through the time interleaving of several high-speed digital-to-analog converters' outputs, to enable the transmission of high order electrical modulation formats (PAM-4, PAM-8) for ultra high capacity (>1Tb/s/channel) optical communications. In this paper, we present the design, fabrication and measurement of an AMUX circuit realized in III-V Lab in-house InP DHBT technology. The design challenges and necessary tradeoffs are discussed. Measurements of PAM-4 AMUX output signals up to 100 GBd with an over 1-V differential output swing are presented.

1 Introduction

The continuous development of new communication services and applications results in important increase of high capacity and high-speed communication networks [1]. Recently over 220 GBaud transmitter using digital multiplexing selector and simple 2-level On-Off Keying (OOK), was reported [2].
However, future generations of optical networks will need interfaces operating beyond Tb/s. To obtain such high network capacity, more complex modulation formats, operating at very high symbol-rate, are intensively investigated. In this context, Pulse Amplitude Modulation (PAM) is of particular interest.
Digital-to-analog converter (DAC) and analog-to-digital converter (ADC) that are mostly based on Si CMOS, face strong analog bandwidth limitations, impacting the performances of optical network transceivers.
Thus, to both alleviate those bandwidth limitations and increase optical network capacity, an analog multiplexing architecture was proposed. It consists in the time interleaving of several high-speed DAC outputs to aggregate their individual bandwidth.
Over the past years, several research works reported increasing performances of analog multiplexers. In [3] an analog multiplexer realized in InP DHBT technology with 25 GHz bandwidth was presented. The authors of [4] report a SiGe HBT analog multiplexer with 67-GHz bandwidth. Finally, in 2019 a 2:1 AMUX with 110-GHz bandwidth realized in InP DHBT process [5], while in [6] 400-Gbs Pulse-Shaped PAM transmission using integrated AMUX-MZM is reported.

In this work, we present the design and fabrication of a 2:1 AMUX integrated circuit realized in InP DHBT technology. Measurements in PAM-4 mode were realized up to 100 GBd conjugated with an over 1-V differential output swing.

2. Technology

The AMUX was fabricated in III-V LAb 0.7-µm emitter width InP DHBT technology, described in [7]. Transistors used in this design have a static current gain of about 30, a breakdown voltage, BV_{CE0}, of more than 4 V, and peak f_T and f_{MAX} of respectively 340 and 410 GHz, at a current density of 6 mA/µm². Recent optimization of the epitaxial layer structure improved transistor thermal resistance and allowed more compact layout. NiCr thin film resistors, Si_3N_4 MIM capacitors and three Au-based interconnect levels are available in the process.

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3. Architecture and design

The Analog Multiplexer bloc diagram is presented in Fig.1. This circuit has three single-ended (SE) inputs (Data1, Data2 and Clock) and one differential output, thus allowing a very compact layout and easing packaging efforts, as all inputs are located on the same die side, as shown on Fig.2 . Each data stream is converted from single-ended to differential and amplified by a two-stage linear amplifier. Differential outputs of these amplifiers are feeding the analog selector core, which is realized as a modified linear Gilbert cell. The clock signal is provided to the AMUX core by an amplifier, which performs the single-ended to differential conversion of the input signal and amplifies it. The output amplifier relies on a cascode stage that implements resistive emitter degeneration to both improve bandwidth and the linear dynamic.

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Different tradeoffs and choices should be done between three important characteristics: linearity, gain and bandwidth. All operation on data (input amplifiers, core, output amplifiers) should be realized in a linear mode to preserve multi-level signals integrity. For a given input signal range and linear gain, the output linear amplitude is then defined. The gain and linear dynamic of each data path stage can then be set to find the optimal sequence while ensuring the required bandwidth for high symbol-rate operation of the AMUX.
In this design, passive peaking is used in data input blocs and core to improve circuit's overall bandwidth. The peaking values were limited in order to avoid overshoots, which could degrade the quality of multilevel signals.

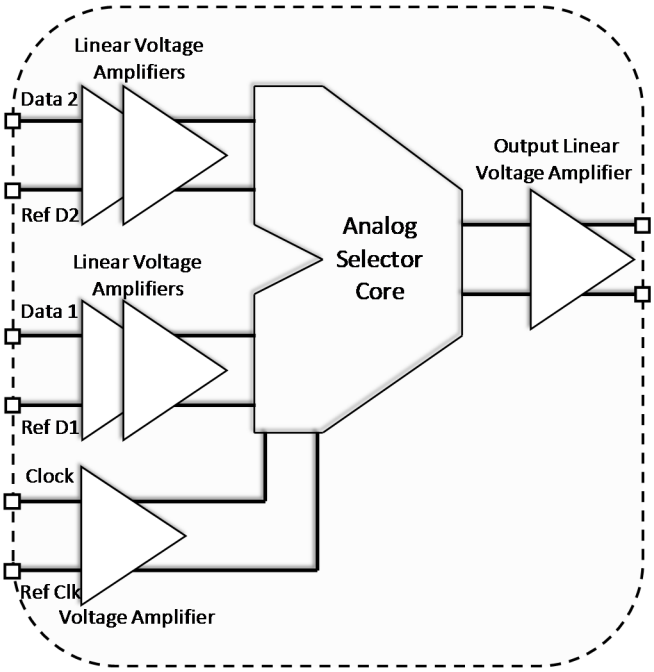

Fig. 1. Bloc diagram of Analog Multiplexer.

The chip footprint is 1.5x1.2 mm^2. Three signal inputs are located at the left side of the chip and the differential output is located on the right side. All inputs and outputs transmission lines are broadband coplanar waveguides. Low ohmic RC-damped decoupling networks have been integrated to ensure a proper biasing of all the AMUX stages.

2. Circuit measurements

Two input data streams, Data1 and Data2, are provided by two de-correlated differential outputs from a high speed packaged DAC. This DAC was fabricated in III-V Lab InP DHBT technology. Clock signals for DACs and for the AMUX are generated by internal clock distribution and synchronized by a 10-MHz reference time base.
In Fig. 3 and 4 PAM-4 measurements at respectively 70 and 100 GBd are presented. Differential output swings of 1.1 and 0.9 V_{pp} have been obtained at respectively 70 and 100 GBd from a 200-mV_{pp} single-ended input. A good eye diagram quality is achieved, although strongly limited by the measurement setup.

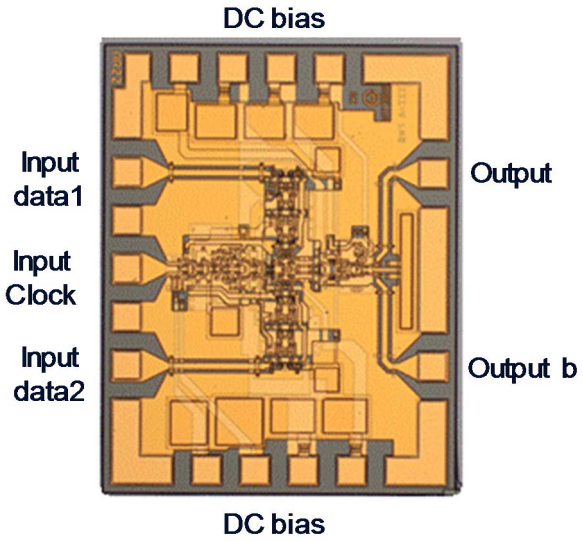

Fig. 2. AMUX die microphotograph

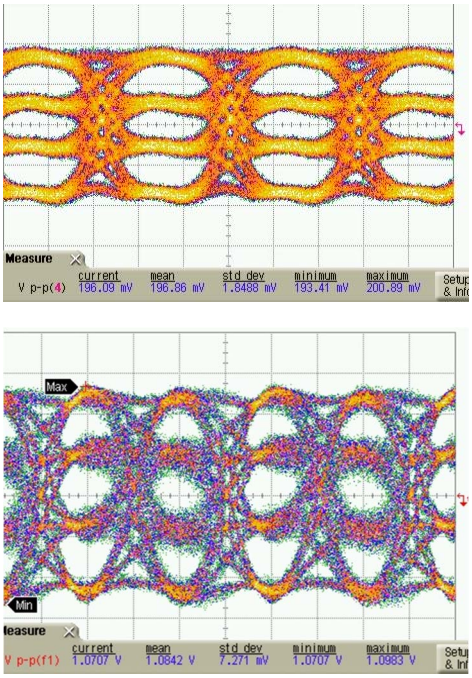

Fig. 3. Top: single-ended input signal at 35 GBd with a 200-mV_{pp} amplitude (50 mV/div, 10 ps/div)
Bottom: differential output signal at 70 GBd with a 1.1-V_{pp} swing (200 mV/div, 7.1ps/div)

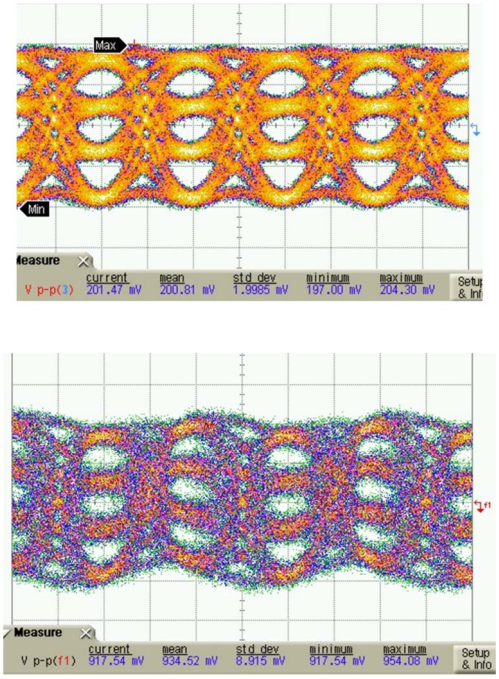

Fig. 4. Top: single-ended input signal at 50 GBd with a 200-mV_{pp} amplitude (50 mV/div, 10 ps/div) Bottom: differential output signal at 100 GBd with a 0.9-V peak-to-peak amplitude (200 mV/div, 5ps/div)

5 Conclusion

This article presents the design and measurements of a 2:1 analog multiplexer integrated circuit, realized in III-V Lab 0.7-µm emitter width InP DHBT technology. PAM-4 measurements at 70 and 100 GBd with 1.1 and 0.9 V_{ppdiff} respectively are reported, showing good performance. Further investigations of the circuit's performances could lead to higher symbol rate measurements and high capacity coherent optical system tranmissions.

6 Acknowledgements

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